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Date <u>09/08/02</u>	Serial # <u>9402</u>	Priority Application Date _____
Your Name <u>M. Lewis</u>	Examiner # _____	
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09-04-02 P03:47 IN

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Teaching Refs _____

What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-6Problem: See Page 4 Lines 10-22

Solution: " " 5 " 2-25
 " " 6 " 1-8

Novelty in Individually illustrated
in claims

Staff Use Only	Type of Search	Vendors
Searcher: <u>Speckhard</u>	Structure (#) _____	STN <input checked="" type="checkbox"/>
Searcher Phone: <u>308-6559</u>	Bibliographic <input checked="" type="checkbox"/>	Dialog <input checked="" type="checkbox"/>
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation _____	Questel/Orbit _____
Date Searcher Picked Up: <u>9/12/02</u>	Fulltext <input checked="" type="checkbox"/>	Lexis-Nexis _____
Date Completed: <u>9/12/02</u>	Patent Family _____	WWW/Internet _____
Searcher Prep/Rev Time: <u>80</u>	Other _____	Other _____
Online Time: <u>120</u>		

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09/12/2002 09/837,397

12sep02 12:19:31 User267149 Session D324.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2002/Sep W2
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*File 94: There is no data missing. UDs have been adjusted to reflect the current months data. See Help News94 for details.
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File 108:AEROSPACE DATABASE 1962-2002/Aug
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File 305:Analytical Abstracts 1980-2002/Aug W4
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File 315:ChemEng & Biotec Abs 1970-2002/Jul
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File 350:Derwent WPIX 1963-2002/UD,UM &UP=200258
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*File 350: Alerts can now have images sent via all delivery methods. See HELP ALERT and HELP PRINT for more info.
File 344:Chinese Patents Abs Aug 1985-2002/Aug
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File 347:JAPIO Oct 1976-2002/May(Updated 020903)
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*File 347: JAPIO data problems with year 2000 records are now fixed.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/12/2002 09/837,397

Alerts have been run. See HELP NEWS 347 for details.

File 371:French Patents 1961-2002/BOPI 200209

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*File 371: This file is not currently updating. The last update is 200209.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/12/2002 09/837, 397

Set	Items	Description
S1	597595	(SEMICONDUCT????? (N1) DEVICE? ?)
S2	2439677	SEMICONDUCT?????
S3	7271	CC=B2560
S4	5052	MC=S01-G02B
S5	99760	IC=G01R-031
S6	2517700	S1:S5
S7	84504	GATE??(3N) (CONDUCT??? OR ELECTRODE? ? OR MICROELECTRODE? ?)
S8	4112853	ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????
S9	408916	(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????) (3N) (LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S10	12074	CC=(B2110 OR B2160 OR B8130)
S11	4753	MC=(S05-A02 OR S05-D01A1A OR U11-C05C4)
S12	7751	IC=(A61N-001/04 OR A61N-001/06 OR A61B-005/04)
S13	4756	MC=(V05-D07C5C OR V07-F01A1)
S14	108566	IC=(H01J-029/89 OR G02B-006)
S15	4225964	S8:S14
S16	230301	(P OR N) () TYPE? ?
S17	1934859	SUBSTRATE? ?
S18	224253	CC=(A6855 OR A8115 OR B0520 OR B2570)
S19	2952	MC=(T03-A01B OR T03-A01B1 OR T03-A01B)
S20	5762	IC=G11B-005/704
S21	2088842	S17:S20
S22	442210	(INSULAT????? OR DIELECTRIC???) (3N) (LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S23	69304	(INSULAT????? OR DIELECTRIC???) (3N) GATE??
S24	12857	MC=(U11-C06A1B OR U11-C07C3 OR U11-C08A1 OR U11-C08A6)
S25	27894	CC=(A5150 OR A7700 OR B2800 OR B2810 OR B2830)
S26	508967	S22:S25
S27	477479	(LOW OR LOWER OR MIDDLE OR HIGH???) (3N) CONCENTRAT??????
S28	7686	(REVERSE? OR BACKWARD) (3N) (ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????)
S29	484884	S27:S28
S30	122379	(DRAIN???? OR SOURCE? ? OR CHANNEL???) (3N) (REGION???? OR AREA????)
S31	79295	(HIGH OR LOW OR LOWER) (3N) (DOPE???? OR DOPA???? OR DOPE?-?? OR DOPA????? OR DOPING OR IMPURIT???????)
S32	80129	(DOPE???? OR DOPA???? OR DOPE???? OR DOPA????? OR DOPING OR IMPURIT???????) (3N) CONCENTRAT??????
S33	140845	S31:S32
S34	61163	S6 AND S7
S35	61163	S34 AND S15
S36	38938	S35 AND S21
S37	23157	S36 AND S26
S38	2312	S37 AND S29
S39	1269	S38 AND S30
S40	782	S39 AND S33
S41	344	S40 AND S16
S42	286	S41 AND S31
S43	274	S42 AND S32
S44	274	S43 AND S27
S45	6	S44 AND S28
S46	6	RD (unique items)

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S47 268 S44 NOT S46
S48 268 S47 AND (S1 OR S2)
S49 268 S48 AND S7
S50 247 S49 AND S22
S51 158 S50 AND S23
S52 139 S51 AND DRAIN???
S53 97 S52 AND (DRAIN???(2N) SOURCE???)
S54 0 S53 AND (SUSTAIN????(3N) (VOLT???? OR POTENTIAL))
S55 24 S53 AND VOLT?????
S56 24 RD (unique items)
S57 24 IDPAT (sorted in duplicate/non-duplicate order)
S58 24 IDPAT (primary/non-duplicate records only)
S59 73 S53 NOT S58
S60 0 S59 AND SPAN??????
S61 2 S59 AND REVERS???(2N) CONDUCT??????
S62 71 S59 NOT S61
S63 71 S62 AND (GATE???(1N) ELECTROD???)
S64 22 S63 AND (CHANNEL? ?(1N) REGION???)
S65 22 RD (unique items)
S66 22 IDPAT (sorted in duplicate/non-duplicate order)

09/12/2002 09/837,397

46/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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04361950

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF AND
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING THE DEVICE

PUB. NO.: 06-005850 [JP 6005850 A]
PUBLISHED: January 14, 1994 (19940114)
INVENTOR(s): MAEDA ATSUSHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 04-157984 [JP 92157984]
FILED: June 17, 1992 (19920617)
JOURNAL: Section: E, Section No. 1534, Vol. 18, No. 199, Pg. 149,
April 07, 1994 (19940407)

ABSTRACT

PURPOSE: To control the decrease or variation in threshold voltage due to a short channel effect accompanying fineness, by forming a **gate electrode** with first and second **electrodes** and forming the second **electrode** in a **conductive type reverse** to the first **electrode** and having a low concentration of **impurity**.

CONSTITUTION: A **gate electrode** 3 through a **gate insulating film** is formed on a **semiconductor substrate** 1 interposed between **source** and **drain** regions 4 installed on a main surface of the **substrate** 1. The **gate electrode** 3 comprises a **first gate electrode** 3b of the center and a **second electrode** 3c. The **second electrode** 3c is installed on the side of the **first gate electrode** 3b, and a **P-type** impurity is introduced into the **second electrode** 3c, and the **second electrode** 3c is formed in a **conductive type reverse** to the **first electrode** 3b into which an **N-type** impurity is introduced. A work function value of the **second electrode** 3c is set larger than that of the **first gate electrode** 3b. Thus, the work function value of the **gate electrode** is large in the proximity of the **second gate electrode** and the decrease in threshold voltage can be controlled.

46/3,AB/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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02005074

MANUFACTURE OF MOSFET

PUB. NO.: 61-219174 [JP 61219174 A]
PUBLISHED: September 29, 1986 (19860929)
INVENTOR(s): SOEJIMA KATSUMOTO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-059952 [JP 8559952]
FILED: March 25, 1985 (19850325)
JOURNAL: Section: E, Section No. 482, Vol. 11, No. 59, Pg. 96,
February 24, 1987 (19870224)

ABSTRACT

PURPOSE: To produce a shortchanneled MOSFET with high withstand voltage by a method wherein silicon oxide film in a part of region along the ends of a **gate electrode** is selectively removed to heat-treat the surface so that the junctions in **source** and **drain regions** in the part near **gate electrode** may be shallowed while reducing the **concentration of reverse conductive impurity**.

CONSTITUTION: A **gate insulating film** 2 is formed on a **P-type** silicon **substrate** 1 and then polycrystalline silicon is deposited on the film 2 to be selectively etched forming a **gate electrode** 3. The **gate insulating film** 2 not covered with the **gate electrode** 3 is removed and overall surface is heat-treated to form a silicon oxide film 4 for implanting it with phosphorus ion. Firstly photoresists 6 are formed along the sides of **gate electrode** 3 making gaps by e in length to selectively remove the silicon oxide film 4 using the photoresists 6 as masks. Secondly the overall surface is heat-treated in nitrogen atmosphere. Finally source drain junctions 13 in **low concentration** can be produced in the regions 8 with the silicon oxide film 4 removed therefrom since the **high concentration impurity** is hardly diffused in the lateral direction.

46/3,AB/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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01934776
CHARGE TRANSFER DEVICE

PUB. NO.: 61-148876 [JP 61148876 A]
PUBLISHED: July 07, 1986 (19860707)
INVENTOR(s): KIMATA MASAAKI
TSUBOUCHI NATSUO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 59-271546 [JP 84271546]
FILED: December 21, 1984 (19841221)
JOURNAL: Section: E, Section No. 457, Vol. 10, No. 347, Pg. 75,
November 21, 1986 (19861121)

ABSTRACT

PURPOSE: To obtain sufficient transfer efficiency at a low temperature, by changing the potential of the **channel region** in the second **conducting type semiconductor** region, which is formed on the first **conducting semiconductor substrate**, in the direction perpendicular to the charge transfer direction.

CONSTITUTION: On a first **conducting type semiconductor substrate** 130, a second **conducting type semiconductor** region 121, in which impurities having the **reverse conducting** type with respect to the first **conducting type**, is formed. A **gate insulating film** 110 is formed on the region 121. A plurality of **gate electrodes** 21, 31, 41, 51, 22, 32, 42 and 52 are formed on the layer 110 so that they are separated one another. The potential of a **channel region** 10 in the second **conducting type semiconductor** region 121 in such a charge transfer device is changed in the direction perpendicular to the charge transfer direction. For example, on the **p type silicon substrate** 130, the **n type** impurity region 121 and an **n type** impurity region 140 having **lower impurity concentration** than the region 121 are alternately arranged in said perpendicular directions. They are shallower than the potential of a thin **n type** impurity region 140.

46/3,AB/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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01794873

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 61-008973 [JP 61008973 A]
PUBLISHED: January 16, 1986 (19860116)
INVENTOR(s): YASUI JURO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company
or Corporation), JP (Japan)
APPL. NO.: 59-129804 [JP 84129804]
FILED: June 22, 1984 (19840622)
JOURNAL: Section: E, Section No. 408, Vol. 10, No. 150, Pg. 19, May
31, 1986 (19860531)

ABSTRACT

PURPOSE: To manufacture the highly reliable **semiconductor device** at a high yield rate, by providing a process, in which impurity ions, which are accelerated approximately vertically with respect to the main surface of a **semiconductor substrate** are implanted into a **semiconductor** film or in the second insulating film, providing a process, in which **reverse conducting** type impurity ions are implanted into the **semiconductor substrate**, thereby forming a side wall in excellent uniformity and reproducibility.

CONSTITUTION: P ions are implanted in a **P type semiconductor substrate** 1, and first source and drain 7 having low impurity concentration are formed. Then an Si(_{sub}3)N(_{sub}4) film 11 is formed. A polycrystalline Si film 12 is formed under the pressure reduced state by a CVD method utilizing the thermal decomposition of Si(_{sub}3)N(_{sub}4). Thereafter, P ions, which are accelerated in the direction approximately vertical to the main surface of the **substrate** 1 are implanted. By using an etching liquid comprising fluoric acid, nitric acid and acetic acid, the **semiconductor** film 12 is etched. The **source** and **drain regions**, in which high-concentration P ions are implanted, and semiconductor films 121 and 122 at the flat part of the surface of a **gate electrode** and the like are removed. When accelerated As ions are implanted, an Si(_{sub}3)N(_{sub}4) film 110 and a polycrystalline Si film 120 are deposited on the side surface of the **gate electrode** 4. Second source and drain 15 having high impurity concentration are formed.

46/3,AB/5 (Item 5 from file: 347)
DIALOG(R) File 347:JAPIO
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00991665

INSULATED GATE TYPE FIELD EFFECT TRANSISTOR

PUB. NO.: 57-141965 [JP 57141965 A]
PUBLISHED: September 02, 1982 (19820902)
INVENTOR(s): KATO KUNIHARU
NAGANO HITOSHI
SHIMADA YUKI
KURODA IWAO
YOSHIDA HIROSHI
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-027294 [JP 8127294]
FILED: February 26, 1981 (19810226)
JOURNAL: Section: E, Section No. 145, Vol. 06, No. 243, Pg. 56,
December 02, 1982 (19821202)

ABSTRACT

PURPOSE: To reduce ON resistance by providing a one **conductive** type source region in a one **conductive** type drain region through two **reverse** conductive type regions to obtain the IGFET, and providing the surface layer part having high impurity concentration in a drain region located between the two **reverse** conductive region.

CONSTITUTION: A **substrate** 3 which is to become the **drain** region is prepared by laminating an N^(sup +) type layer 2 and an N^(sup -) type layer 1. A drain **electrode** M4 is deposited on the entire back surface of the layer 2. Then two **P type** regions Z1 are diffused and formed in the layer 1. Z3 which is to become a source region is provided in each region. A **source** electrode M1 is attached on the area from the central part of each region Z3 and to the outer edge part of each region 1. A **gate** electrode M2 which faces the M1 is provided on the area from each region Z3 to the edge of each region Z1 through a **gate** insulating film 5. Thus the FET is obtained. In this constitution, only the surface layer part of the layer 1 between the region Z1's is transformed into an N^(sup +) type region 25, the ON resistance is decreased, and the IGFET with low power consumption is obtained.

46/3,AB/6 (Item 6 from file: 347)
DIALOG(R) File 347:JAPIO
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00753168

MOS TYPE SEMICONDUCTOR DEVICE

PUB. NO.: 56-073468 [JP 56073468 A]
PUBLISHED: June 18, 1981 (19810618)
INVENTOR(s): DAN RONBO
IWAI HIROSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 54-149948 [JP 79149948]
FILED: November 21, 1979 (19791121)
JOURNAL: Section: E, Section No. 72, Vol. 05, No. 137, Pg. 122, August
29, 1981 (19810829)

ABSTRACT

PURPOSE: To control punching-through currents by a method wherein an impurity buried region in a conduction type reverse to the impurities of a substrate is formed in the substrate being located at fixed depth from the interface between a gate insulating film and the substrate.

CONSTITUTION: An MOS type semiconductor device is formed in such a manner that N^(sup +) type source and drain regions 12, 12' are diffusion-formed to a P type Si substrate 11, a gate insulating film 13 is coated over a channel region of the intermediate exposing substrate 11 from the end sections of these regions, and a gate electrode 14 is attached on the film 13. In this constitution, a high concentration impurity buried region 16 in a conduction type reverse to the impurities of the substrate is previously made up in the substrate 11 at fixed depth from the interface 15 between the substrate 11 and the gate insulating film 13. Thus, punching-through currents can be inhibited because a depletion layer pushes up elongation current carriers to the interface on the basis of the inverse bias of a junction generated between the region 16 and the substrate 11. And threshold value voltage does not change.

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58/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014622483
WPI Acc No: 2002-443187/200247
XRAM Acc No: C02-126105
XRPX Acc No: N02-349126

Flat panel display device comprises thin film **semiconductor** switching element, display **electrode**, **dielectric layer** formed on surface of **semiconductor** layer, and metal layer on surface of the **dielectric layer**

Patent Assignee: JADA N (JADA-I); YOSHIHASHI H (YOSH-I)

Inventor: JADA N; YOSHIHASHI H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020039814	A1	20020404	US 2001964403	A	20010928	200247 B

Priority Applications (No Type Date): JP 2001102451 A 20010330; JP 2000300833 A 20000929

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20020039814	A1	27	H01L-021/00	

Abstract (Basic): US 20020039814 A1

Abstract (Basic):

NOVELTY - Flat panel display device has a thin film **semiconductor** switching element on a surface of a **substrate**, a display **electrode** connected with the switching element, a **semiconductor** layer for auxiliary capacity which is electrically connected with the display **electrode**, a **dielectric layer** formed on a surface of the **semiconductor** layer, and metal layer on surface of the **dielectric layer**.

DETAILED DESCRIPTION - Flat panel display device comprises a thin film **semiconductor** switching element formed on a surface of a **substrate**, a display **electrode** connected with the switching element, a **semiconductor** layer for auxiliary capacity which is electrically connected with the display **electrode**, a **dielectric layer** formed on a surface of the **semiconductor** layer for auxiliary capacity, and a metal layer formed on a surface of the **dielectric layer**. The auxiliary capacity is constituted by the **semiconductor** layer for auxiliary capacity, the **dielectric layer**, and the metal layer; and the switching element includes a **channel region**, and a **semiconductor** layer having **source** and **drain** regions disposed to sandwich the **channel region** between them and implanted respectively with an **n-type** or **p-type** impurity ion. The **impurity** having the same concentration as the **impurity** ion implanted into the **source/drain regions** is implanted into the **semiconductor** layer for auxiliary capacity in the same step. A surface concentration of the **n-type** or **p-type** impurity ion is 3.2×10^{19} to 2×10^{20} atoms/cm³. An INDEPENDENT CLAIM is also included for a method of manufacturing a flat panel display

device, which comprises depositing a layer of the **semiconductor** switching element on the **substrate** concurrent with a deposition of the **semiconductor** layer for auxiliary capacity on the **substrate**; forming a mask pattern covering a region of the switching element which is subsequently turned into a **channel** region but exposing entire surfaces of **source/drain** regions of the switching element and of the **semiconductor** layer of auxiliary capacity; implanting an impurity ion through the mask pattern into entire surfaces of **source/drain** regions of the switching element and of the **semiconductor** layer for auxiliary capacity; and depositing a metal layer and subjecting it to a patterning process to form a **gate electrode** of the switching element and an auxiliary capacity line facing the **semiconductor** layer for auxiliary capacity.

USE - As flat panel display device.

ADVANTAGE - The inventive device minimizes **voltage** dependency of the auxiliary capacity, thus making it possible to achieve a normal display even if a driving **voltage** is low. It minimizes point defects to be generated due to a deterioration of the **dielectric layer**, thus exhibiting excellent quality and reliability.

DESCRIPTION OF DRAWING(S) - The figures show a graph illustrating the C-V characteristics of the auxiliary capacity of liquid crystal display device, and a cross-sectional view schematically illustrating the step of implanting a **high concentration of impurity** into a **semiconductor** layer of auxiliary capacity.

pp; 27 DwgNo 1, 2/14

58/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013873731
WPI Acc No: 2001-357943/200138
XRAM Acc No: C01-111088
XRPX Acc No: N01-260208

Semiconductor device, e.g., dynamic threshold voltage metal oxide **semiconductor** field effect transistor, has **channel region** made of first **semiconductor** and body region made of second **semiconductor** of second conductivity type

Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)

Inventor: INOUE A; TAKAGI T

Number of Countries: 027 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1102327	A2	20010523	EP 2000124837	A	20001114	200138 B
JP 2001210831	A	20010803	JP 2000341732	A	20001109	200150

Priority Applications (No Type Date): JP 99324009 A 19991115

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 1102327 A2 E 57 H01L-029/78

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

JP 2001210831 A 31 H01L-029/786

Abstract (Basic): EP 1102327 A2

Abstract (Basic):

NOVELTY - A **semiconductor device** has **gate electrode** provided on a **gate insulator film**; **source** and **drain region** of first conductivity type; a **channel region** made of first **semiconductor** and provided between the **source** and **drain regions**; a **body region** made of a second **semiconductor** of second conductivity type and provided below the **channel region**; and a **conductor member**.

DETAILED DESCRIPTION - A **semiconductor device** comprises: a **substrate** (10); a **semiconductor layer** (30) in part of the **substrate**; a **gate insulator film** (16) on the **semiconductor substrate**; a **gate electrode** (17) on the **insulator film**; a **source** and **drain regions** of a first conductivity type on both sides of **gate electrode regions**; a **channel region** (24) between the **source** and **drain regions** of the **semiconductor layer**; a **body region** (22) below the **channel**; and a **conductor member** (23) for connecting the **gate electrode** and the **body region**. The **channel region** is made of a first **semiconductor**, while the **body region** is made of a second **semiconductor** of a

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second conductivity type having larger potential than that of the first. This larger potential is for carriers at a band edge where carriers travel.

USE - Used as dynamic threshold **voltage** metal oxide **semiconductor** field effect transistor (DTMOS) or metal insulator **semiconductor** field effect transistor (MISFET).

ADVANTAGE - The device has low threshold **voltage**, can operate at high speed, and has a wide operation range.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a high-DTMOS.

Substrate (10)

Gate insulator film (16)

Gate electrode (17)

Body region (22)

Conductor member (23)

Channel region (24)

Cap layer (25)

Semiconductor layer (30)

pp; 57 DwgNo 4/42

09/12/2002 09/837,397

58/3,AB/4 (Item 4 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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012395143
WPI Acc No: 1999-201250/199917
XRPX Acc No: N99-149077

MIS transistor structure of **semiconductor IC device** -
includes **drain** and low resistance **areas** which prolong from
edge of potential controlled domains, so that length of **channel**
areas attain predetermined value
Patent Assignee: HITACHI LTD (HITA); HITACHI MICON SYSTEM KK (HITA-N)
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11045997	A	19990216	JP 97202722	A	19970729	199917 B

Priority Applications (No. Type Date): JP 97202722 A 19970729

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11045997	A	18		H01L-029/78	

Abstract (Basic): JP 11045997 A

NOVELTY - The **drain areas** and low resistance areas
(5Nd2,5Pd2) prolong from the edge of the potential controlled domains,
so that the length of the **channel areas** attain a
predetermined value. DETAILED DESCRIPTION - Potential controlled
domains (5Np,5Pp) which are formed below **gate electrodes**
(5Ngs,5Nps) surrounding a **source area** (5Ns,5Ps) of an

N-type MOSFET (5N) and a **P-type** MOSFET (5P).

Channel areas (5Nc,5Pc) formed below one **gate**
electrodes contain impurity whose conductivity is opposite to
that in the **source areas** and similar to that in **drain**
areas (5Nd1,5Pd1) and have **impurity concentration**
lower than that in the **drain areas**. The **source**
and **drain areas** which are mutually separated, are formed on
both sides of **gate electrode** formed in the upper portion of
a **semiconductor substrate** (1) through a **gate**
insulating film. An INDEPENDENT CLAIM is included for
semiconductor IC device manufacturing method.

USE - For **semiconductor IC device**.

ADVANTAGE - Prevents fault, punch through during setting up of
threshold **voltage**. Reduces **impurity concentration** of
the **substrate** and **drain diffusion capacitance**, thus
improving operational reliability and operation speed of the IC device.

DESCRIPTION OF DRAWING(S) - The drawing shows the sectional view of
principal part of the **semiconductor IC device**. (1)

Semiconductor substrate(5P,5N) **P-type** and

N-type MOSFETS; (5Ns,5Ps) **Source areas**;

(5Nd1,5Pd1) **Drain areas**; (5Nd2,5Pd2) Low resistance areas;

(5Ng,5Pg) **Gate electrodes**; (5Np,5Pp) Potential controlled
domains.

Dwg.1/21

58/3,AB/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO
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02464962

INSULATED-GATE BIPOLAR TRANSISTOR

PUB. NO.: 63-081862 [JP 63081862 A]
PUBLISHED: April 12, 1988 (19880412)
INVENTOR(s): TAGAMI SABURO
APPLICANT(s): FUJI ELECTRIC CO LTD [000523] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-226871 [JP 86226871]
FILED: September 25, 1986 (19860925)
JOURNAL: Section: E, Section No. 650, Vol. 12, No. 318, Pg. 67, August 29, 1988 (19880829)

ABSTRACT

PURPOSE: To prevent ratching without increasing gate threshold voltage by providing a **high impurity concentration** region which is the same conductivity type to a collector region in the collector **region** directly under a **source region**.

CONSTITUTION: The **low impurity concentration** and a conductivity type, n^(sup +) type, second **region (drain or source region)** 2 is provided on the first region (emitter region) 1 made of a p^(sup +)-type **substrate** and the p-type third region (collector region) 3 is selectively formed on the surface of the second region 2. Further, the **high impurity concentration** n^(sup +)-type fourth **region (source region)** 4 is selectively formed on the surface of the third region 3. A **gate electrode** 6 is provided on the fourth region 4 by interposing an **insulating film** 5 (**gate insulating film**). A **collector electrode** 7, an **emitter electrode** 8 and a **p-type high impurity concentration layer** 9 are also provided. A **high impurity concentration** region 10 which is the same conductivity type to the third region 3 is formed directly under the fourth region 4 in the third region 3 by such a method as to implant a **high energy p-type ion** by using the **insulating film** 5 which is used for forming the fourth region 4 as a mask before the **gate electrode** 6 and the **collector electrode** 7 are provided.

09/12/2002 09/837,397

58/3,AB/2 (Item 2 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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014346465
WPI Acc No: 2002-167168/200222
XRAM Acc No: C02-051723
XRXPX Acc No: N02-127871

Silicon-on-insulator metal oxide **semiconductor** field effect transistor has **high density impurity** areas having **impurity concentration higher than substrate**, formed under **p-type source and drain areas**

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001284590	A	20011012	JP 200099497	A	20000331	200222 B

Priority Applications (No Type Date): JP 200099497 A 20000331

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001284590	A	10	H01L-029/786	

Abstract (Basic): JP 2001284590 A

Abstract (Basic):

NOVELTY - Silicon-on-insulator metal oxide **semiconductor** field effect transistor has **high density impurity** areas having **impurity concentration higher than substrate**, formed under **p-type source and drain areas**.

DETAILED DESCRIPTION - Silicon on insulator (SOI) **layer** having **n-type source, drain and channel areas** (106-108), are formed on **insulating film** (105) on **p-type substrate** (101). **Gate electrode** (110) is formed on **gate insulating film** (109) on **channel area**. **n-type impurity area** (104) is formed directly below **channel area** (108). **High density p-type impurity areas** (102, 103) having **impurity concentration higher than substrate**, are formed under **source-drain areas**.

An INDEPENDENT CLAIM is also included for silicon-on-insulator metal oxide **semiconductor** field effect transistor manufacturing method.

USE - Silicon-on-insulator metal oxide field effect transistor (MOSFET).

ADVANTAGE - The thickness of **insulating layer** existing between the **substrate** and SOI layer is reduced to minimum. Reverse short channel effect of SOI layer is reduced by the **impurity concentration on semiconductor substrate** surface, hence a stable threshold **voltage** is maintained.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of SOI MOSFET.

09/12/2002 09/837,397

P-type semiconductor substrate (101)
High density p-type impurity areas (102,
103)
n-type impurity area (104)
Insulating film (105)
N-type source area (106)
N-type drain area (107)
N-type channel area (108)
Gate insulating film (109)
Gate electrode (110)
pp; 10 DwgNo 1/7

09/12/2002 09/837,397

58/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012035372
WPI Acc No: 1998-452282/199839
XRPX Acc No: N98-353188

Lateral double diffused MOSFET for electric power conversion IC -
includes **N type semiconductor** layer in which
impurity concentration between **lower portion of**
drain electrode, well area and drain area
is lower than that in other locations

Patent Assignee: MATSUSHITA ELECTRIC WORKS LTD (MATW)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10189983	A	19980721	JP 96344777	A	19961225	199839 B

Priority Applications (No Type Date): JP 96344777 A 19961225

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10189983	A	12		H01L-029/786	

Abstract (Basic): JP 10189983 A

The MOSFET includes a **semiconductor substrate** (1) on which an **N type semiconductor** layer (3) is formed via an **insulating layer** (2). An **N+ type drain area** (4) is formed on the **N type semiconductor** layer. A **P type well area** (5) is formed at the sides of the **N type semiconductor** layer. An **N+ type source area** (6) is also formed on the surface of the **N type semiconductor** layer. An **insulated gate** (8) is formed on the **P type well area** via the **insulating film**. The **insulated gate** is interposed between the **drain area** and the **source area**.

A **drain electrode** (9) is electrically connected with the **drain area**. A **source electrode** is electrically connected with the **source area**. A **gate electrode** is electrically connected with the **insulated gate**. The **impurity concentration** between the **lower portion of the drain electrode, the well area and the drain area**, is lower than that in other locations. The concentration increases uniformly towards the direction of the **well area** and the **drain area**.

ADVANTAGE - Prevents reduction in breakdown **voltage**.

Dwg.1/9

58/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011810116
WPI Acc No: 1998-227026/199820
XRPX Acc No: N98-180509

Horizontal CMOS-FET manufacturing method for level shift circuit of high side switch driving system - involves forming epitaxial layer and electric field reduction area whose impurity densities are $2.5 \times 10^{12} \text{ cm}^{-2}$ or $4 \times 10^{12} \text{ cm}^{-2}$ and $1 \times 10^{12} \text{ cm}^{-2}$ or $3 \times 10^{12} \text{ cm}^{-2}$, respectively

Patent Assignee: MATSUSHITA ELECTRIC WORKS LTD (MATW)

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10070268	A	19980310	JP 96225681	A	19960827	199820 B
JP 3202927	B2	20010827	JP 96225681	A	19960827	200152

Priority Applications (No Type Date): JP 96225681 A 19960827

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10070268	A	6		H01L-029/78	
JP 3202927	B2	7		H01L-029/78	Previous Publ. patent JP 10070268

Abstract (Basic): JP 10070268 A

The method involves forming a couple of electrically conductive epitaxial layers (2) on the upper part of the main surface of a P-type semiconductor substrate (1). Electrically conductive N-type drain and source areas (6,4) are formed separately in the second epitaxial layer. An electrically conductive P-type channel formation area is formed in the first epitaxial layer, surrounding the source area. An electrically conductive electric field reduction area (10) comprising P-type low impurity concentration part is formed on the main surface of the first epitaxial layer, between the channel formation area and drain area.

A gate electrode (5) is formed in the channel formation area interposed between the source area and epitaxial layer, through a gate insulating film. The impurity density of epitaxial layer is $2.5 \times 10^{12} \text{ cm}^{-2}$ or $4 \times 10^{12} \text{ cm}^{-2}$ and that of the electric field reduction area is $1 \times 10^{12} \text{ cm}^{-2}$ or $3 \times 10^{12} \text{ cm}^{-2}$.

ADVANTAGE - Increases breakdown voltage of semiconductor device. Reduces size of device, considerably.

Dwg.1/4

58/3, AB/7 (Item 7 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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010982083
WPI Acc No: 1996-479032/199648
XRPX Acc No: N96-403987

Power MOS-gated **semiconductor device** - has n+ region with
higher impurity concentration formed in n- region
semiconductor layer, impurities taken into wafer during mfr.
causing contaminant impurities in proximity of concavity of layer surface
are reduced

Patent Assignee: NIPPONDENSO CO LTD (NPDE)

Inventor: KATAOKA M; OKABE N; YAMAMOTO T

Number of Countries: 005 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 740352	A2	19961030	EP 96106547	A	19960425	199648	B
JP 8298266	A	19961112	JP 95102341	A	19950426	199704	
EP 740352	A3	19971008	EP 96106547	A	19960425	199813	
US 5925911	A	19990720	US 96638374	A	19960426	199935	

Priority Applications (No Type Date): JP 95102341 A 19950426

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 740352 A2 E 11 H01L-029/78

Designated States (Regional): DE FR IT

JP 8298266 A 6 H01L-021/336

EP 740352 A3 H01L-029/78

US 5925911 A H01L-029/76

Abstract (Basic): EP 740352 A

The device includes a **N type semiconductor substrate** (1) with two mutually opposing surfaces and a **N type semiconductor layer** (2) with a **lower impurity concentration** than the **substrate** contacting one surface of the **substrate**. In it is a concavity formed by the formation of a local oxide film, in contact with a body region (4).

A **N type source region** (5) is located in the body defining a **channel region** along the body at the side of the concavity. A **gate electrode** (7) is positioned over the channel with a **gate insulating film** (6) between them. A **source electrode** (9) is connected to the body and **source regions**. A **high concentration** region is located in the region of the concavity, the body and the source.

USE/ADVANTAGE - For vertical or lateral metal oxide **semiconductor** field effect transistor and vertical or lateral **insulated gate** bipolar transistor. Suppresses occurrence of defects in LOCOS oxidation or in heat treatment operation. Stops leakage and degradation of breakdown **voltage** between **drain** and **source** as result of defect in **channel region**.

Dwg.1/13

09/12/2002 09/837,397

58/3,AB/8 (Item 8 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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010705341

WPI Acc No: 1996-202296/199621

Related WPI Acc No: 1994-103266; 2002-207696; 2002-207697; 2002-207698;
2002-228915; 2002-228916

XRPX Acc No: N96-169744

Transistor mfr. method for bipolar, CMOS and DMOS - by forming MOS
transistor gate isolated from **channel region** and adjusting
threshold **voltage** by putting dopants into the **channel**
region with implant energy enough to penetrate gate to implant into
channel region

Patent Assignee: SILICONIX INC (SILI-N)

Inventor: CHEN J W; CORNELL M E; WILLIAMS R K; YILMAX H; CHEN W; YILMAZ H

Number of Countries: 005 Number of Patents: 011

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 708482	A2	19960424	EP 95116353	A	19951017	199621	B
US 5541123	A	19960730	US 92948276	A	19920921	199636	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95463647	A	19950605		
US 5541125	A	19960730	US 92948276	A	19920921	199636	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95463165	A	19950605		
US 5547880	A	19960820	US 92948276	A	19920921	199639	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95464978	A	19950605		
US 5559044	A	19960924	US 92948276	A	19920921	199644	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
JP 8227945	A	19960903	JP 95293438	A	19951017	199645	
US 5583061	A	19961210	US 92948276	A	19920921	199704	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95464435	A	19950605		
US 5618743	A	19970408	US 92948276	A	19920921	199720	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95463417	A	19950605		
EP 708482	A3	19970326	EP 95116353	A	19951017	199728	
US 5643820	A	19970701	US 92948276	A	19920921	199732	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95463403	A	19950605		
			US 96667219	A	19960619		
US 5648281	A	19970715	US 92948276	A	19920921	199734	
			US 94226419	A	19940411		

09/12/2002 09/837,397

US 94323950	A 19941017
US 95463137	A 19950605
US 96647073	A 19960508

Priority Applications (No Type Date): US 94323950 A 19941017; US 92948276 A 19920921; US 94226419 A 19940411; US 95463647 A 19950605; US 95463165 A 19950605; US 95464978 A 19950605; US 95464435 A 19950605; US 95463417 A 19950605; US 95463403 A 19950605; US 96667219 A 19960619; US 95463137 A 19950605; US 96647073 A 19960508

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 708482	A2	E	70 H01L-021/8249	Designated States (Regional): DE IT NL
US 5541123	A	67	H01L-021/265	Cont of application US 92948276 CIP of application US 94226419 Div ex application US 94323950 CIP of patent US 5426328
US 5541125	A	67	H01L-021/265	Cont of application US 92948276 CIP of application US 94226419 Div ex application US 94323950 CIP of patent US 5426328
US 5547880	A	66	H01L-021/04	Cont of application US 92948276 CIP of application US 94226419 Div ex application US 94323950 CIP of patent US 5426328
US 5559044	A	66	H01L-021/265	Cont of application US 92948276 CIP of application US 94226419 CIP of patent US 5426328
JP 8227945	A	44	H01L-021/8249	Cont of application US 92948276
US 5583061	A	67	H01L-021/265	CIP of application US 94226419 Div ex application US 94323950 CIP of patent US 5426328
US 5618743	A	66	H01L-021/265	Cont of application US 92948276 CIP of application US 94226419 Div ex application US 94323950 CIP of patent US 5426328 Div ex patent US 5559044
EP 708482	A3		H01L-021/8249	Cont of application US 92948276
US 5643820	A	67	H01L-021/70	CIP of application US 94226419 Div ex application US 94323950 Cont of application US 95463403 CIP of patent US 5426328 Div ex patent US 5559044
US 5648281	A	69	H01L-021/265	Cont of application US 92948276 CIP of application US 94226419 Div ex application US 94323950 Cont of application US 95463137 CIP of patent US 5426328 Div ex patent US 5559044

Abstract (Basic): EP 708482 A

The method involves forming a MOS transistor gate (351) overlying

and isolated (357) from a **channel region** (360) on an **N-type substrate** (42). A **P-type source region** (352) is formed. The transistor threshold voltage is adjusted by implanting **P+type** dopants into the **channel region** at an implant energy such that the dopants penetrate the gate to implant into the **channel region**.

The dopants change the threshold voltage. The adjustment is made after forming a diffused body (308) or base region (310) of another transistor in the same **substrate** to prevent the dopants in the **channel region** from being subjected to diffusion.

USE/ADVANTAGE - Simultaneously forms bipolar transistors, high **voltage** and low **voltage** CMOS transistors, DMOS transistors, zener diodes, and thin film resistors or any desired combination on same integrated circuit chip.

29a,b,c/35

Abstract (Equivalent): US 5648281 A

A method for forming an isolation structure and a bipolar transistor on a **substrate** layer, said **substrate** layer being of a **semiconductor** material of a first conductivity type, comprising the steps of:

doping a first area on an upper surface of said **substrate** layer with dopants of a second conductivity type opposite said first conductivity type to form a first buried region;

doping a second area of said upper surface of said **substrate** layer with dopants of said first conductivity type to form a second buried region, said second area being smaller than said first area, said second area being contained within said first area;

forming an epitaxial layer over said upper surface of said **substrate** layer, said epitaxial layer being of a **semiconductor** material of said second conductivity type, said epitaxial layer having an upper surface;

extending a well region of said first conductivity type into said epitaxial layer from said upper surface of said epitaxial layer, said well region being disposed at least partly over said second area, said well region having a bottom surface which contacts said second buried region, said second buried region being formed by said dopants of said first conductivity type which doped said second area;

forming a first contact region of said second conductivity type, more highly doped than said epitaxial layer, extending from said upper surface of said epitaxial layer and contacting said first buried region, wherein said first contact region surrounds said well region;

implanting ions of said second conductivity type into a base region of said well region at a first energy and first dosage to form a base region of said bipolar transistor;

implanting ions of said second conductivity type into said base region at a second energy, less than said first energy, and with a second dosage, greater than said first dosage, to provide a low resistivity surface **doping** of said base region of said bipolar transistor; and

implanting ions of said second conductivity type into said base region at a third dosage greater than said second dosage to create a base contact region at a top surface of said base region of said bipolar transistor to enable ohmic contact between a metal layer

contacting said base contact region and said base region of said bipolar transistor.

Dwg.28/35US 5643820 A

A method for fabricating an MOS capacitor, said process comprising the steps of:

implanting ions of a first conductivity type into an upper surface of an epitaxial layer of a second conductivity type, prior to any **gate dielectric layer** being formed on said upper surface, to form a highly doped first region of said first conductivity type, said first region being implanted with ions of said first conductivity type with a dose of approximately 1E15 cm² or greater, said step of implanting also forming a separate zener diode region in said epitaxial layer;

forming a **gate dielectric layer** overlying said first region and overlying one or more **channel regions** for MOS transistors to be formed; and

forming a **conductive polysilicon layer** overlying said **gate dielectric layer** and overlying said first region and said **channel regions** such that said **conductive polysilicon layer** is separated from said first region and said **channel regions** by said **gate dielectric layer**, wherein said first region and said **conductive polysilicon layer** form two plates of said MOS capacitor.

Dwg.31/35

US 5618743 A

A method for forming an MOS transistor in conjunction with transistors of a different type in the same **substrate** comprising the steps of:

forming a gate of said MOS transistor overlying and isolated from a **channel region** of a **semiconductor** material of a first conductivity type;

forming a **source region** of a second conductivity type lowering a threshold **voltage** of said MOS transistor by implanting dopants of said second conductivity type into said **channel region** in said **semiconductor** material at an implant energy such that said dopants of said second conductivity type penetrate said gate to implant into said **channel region** underlying said gate, said **dopants** being sufficient to lower a threshold **voltage** of said MOS transistor to achieve a desired threshold so that said MOS transistor is capable of being selectively controlled to change between a **conductive** state and a nonconductive state,

said step of lowering a threshold **voltage** of said MOS transistor occurring after a diffusion step for forming a diffused body or base region of another transistor in said same **substrate** to prevent said dopants of said second conductivity in said **channel region** from being subjected to said diffusion step,

wherein said step of forming said **source region** comprises patterning a photoresist masking layer overlying said **semiconductor** material and depositing dopants of said second conductivity type into exposed portions of said **semiconductor** material, and wherein said step of lowering a threshold **voltage** is conducted while said photoresist masking layer remains overlying said **semiconductor** material so that said step of

lowering said threshold **voltage** does not require another masking step.

29b,c/35

US 5583061 A

A method for forming at least two PMOS transistors having different intended breakdown **voltages**, said method comprising the steps of:

forming a first gate of a first PMOS transistor, said first gate having a length of approximately 2 microns to achieve a first breakdown **voltage**;

forming a second gate of a second PMOS transistor, said second gate having a length of approximately 2.5 microns to achieve a higher breakdown **voltage** than said first breakdown **voltage**;

implanting **P-type** dopants at a first energy and a first dosage using a first mask to form **source** and **drain** regions for said first PMOS transistor and said second PMOS transistor, said first energy being insufficient to cause said dopants to penetrate through said gate, said **source** and **drain** regions being self-aligned with said first gate and said second gate; and

implanting **P-type** dopants through said first gate and said second gate at a second energy higher than said first energy and a second dosage lower than said first dosage to adjust a threshold **voltage** of said first PMOS transistor and said second PMOS transistor such that said first PMOS transistor and said second PMOS transistor are formed using the same process steps, said step of implanting **P-type** dopants through said first gate and said second **gate** being **conducted** using said first mask.

29A,29C/35

US 5559044 A

A method for forming a DMOS transistor and a bipolar transistor in a same **substrate** comprising the steps of:

forming a gate of said DMOS transistor overlying said **substrate**;

implanting ions of a first conductivity type into a first region of a **semiconductor** material of a second conductivity type at a first energy and dosage;

driving in said ions of said first conductivity type to form a body of said DMOS transistor, said body being formed so as to cause said DMOS transistor to have desired operating characteristics;

implanting said ions of said first conductivity type into a second region of said **semiconductor** material at a second energy and second dosage, said second energy being less than said first energy, said step of implanting said ions into said second region being **conducted** after the formation of said body of said DMOS transistor;

driving in said ions of said first conductivity type in said second region to form a base region of said bipolar transistor, said base region being shallower and more highly doped than said body to provide said bipolar transistor with desired operating characteristics;

implanting ions of said first conductivity type into said second region at a third energy, less than said second energy, and with a third dosage, greater than said second dosage, to provide a low resistivity surface **doping** of said base region of said bipolar

transistor; and

implanting ions of said first conductivity type into said second region at a fourth dosage greater than said third dosage to create a base contact region at a top surface of said base region of said bipolar transistor to enable ohmic contact between a metal layer contacting said base contact region and said base region of said bipolar transistor.

Dwg.27/35

US 5547880 A

A method for forming a zener diode region and an isolation region comprising the steps of:

forming an isolation region of a first conductivity type extending from a first surface area of an epitaxial layer of a second conductivity type and contacting a **semiconductor** material of said first conductivity type located below said first surface area, said isolation region having a first **impurity concentration**; and

implanting ions of said first conductivity type into a second surface area of said epitaxial layer, after said step of forming an isolation region, to form a zener diode region of said first conductivity type in said second surface area for use in forming a zener diode having a selected reverse breakdown **voltage**, said zener diode region having a second **impurity concentration** higher than said first **impurity concentration**,

said step of implanting also including implanting said ions in said first surface area to additionally dope said isolation region.

Dwg.31/35

US 5541125 A

A method for forming a lateral MOS transistor having a lightly doped **drain** for increased breakdown **voltage** and for forming other transistors in the same **substrate**, said method comprising the steps of forming a first gate for a lateral MOS transistor and a second gate for a DMOS transistor overlying and insulated from a **semiconductor** material;

forming a first masking layer over said **semiconductor** material to mask a first area around said first gate and expose a second area around said second gate;

implanting ions of a first conductivity type into said second area using said second gate and said first masking layer as a mask for forming a self-aligned body region of said first conductivity type for said DMOS transistor;

removing said first masking layer to expose said first area around said first gate and expose said second area around said second gate;

implanting ions of a second conductivity type into said first area and said second area, said first gate and said second gate acting as a mask to self-align implantation of said ions of said second conductivity type with said first gate and said second gate, said ions of said second conductivity type counter-doping said body region of said DMOS transistor and forming a lightly doped **drain** of said lateral transistor self-aligned with said first gate,

said step of implanting said ions of said first conductivity type being adjusted to take into account said counter-doping from said implantation of said ions of said second conductivity type into said body region so that said body region has desired electrical

characteristics;

forming a second masking layer over a portion of said lightly doped **drain** to leave an exposed portion of said lightly doped **drain**; and

implanting ions of said second conductivity type into said body **region** to form a **source region** of said DMOS transistor and into said exposed portion of said lightly doped **drain** to form a **drain region** of said lateral MOS transistor spaced from said first gate.

Dwg.15a/35

US 5541123 A A method for forming a bipolar transistor to achieve a selected breakdown **voltage** comprising the steps of:

forming a base region of a first conductivity type in a **semiconductor** material of a second conductivity type;

forming a collector contact region of a second conductivity type in said **semiconductor** material of said second conductivity type;

forming a base contact region of said first conductivity type in said base region, said base contact region being more highly doped than said base region, said base contact region being spaced from a closest edge of said base region so as to increase a distance between said base contact region and said collector contact region, said distance being sufficient to avoid breakdown between said base contact region and said collector contact region through said **semiconductor** material of said second conductivity type; and

forming a first region of said second conductivity type, but more lightly doped than said collector contact region, between said collector contact region and said base region to increase a breakdown **voltage** between said base contact region and said collector contact region,

wherein said collector contact region and said first region surround said base region at a surface of said **semiconductor** material.

Dwg.33/35

58/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004505126
WPI Acc No: 1986-008470/198602
XRAM Acc No: C86-003551
XRPX Acc No: N86-006079

Complementary misfet - have **source** and **drain regions**
formed using **gate electrodes** with sidewalls as masks and
shallow **N-type** region formed before forming sidewalls

Patent Assignee: HITACHI LTD (HITA)

Inventor: KOYANAGI M

Number of Countries: 007 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 166167	A	19860102	EP 85106024	A	19850515	198602	B
JP 60241256	A	19851130	JP 8496462	A	19840516	198603	
US 4891326	A	19900102	US 88206896	A	19880608	199009	
EP 166167	B	19911113				199146	
DE 3584644	G	19911219				199201	
KR 9303456	B1	19930429	KR 853089	A	19850507	199421	

Priority Applications (No Type Date): JP 8496462 A 19840516

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 166167 A E 18

Designated States (Regional): DE FR GB IT

EP 166167 B

Designated States (Regional): DE FR GB IT

KR 9303456 B1 H01L-027/08

Abstract (Basic): EP 166167 A

A CMOS **semiconductor device** comprises a first type **substrate** (1) contg. a second type well region (2); and a MISFET in each of the **substrate** and well, each having a **gate electrode** (8) and a **source/drain region** to form a p-channel MISFET and an n-channel MISFET. The **source/drain region** of the p-channel MISFET is a single **p type region** (22). The **source/drain region** of the n-channel MISFET consists of a first **n type region** (18) sep'd. from the **gate electrode** and a second **n type region** (15) between the first region and the **gate electrode** which is shallower than the first region and has **lower impurity concn.**

The device is mfd. in the **substrate** and well by (a) forming a **gate electrode** for each MISFET; (b) introducing **n-** **type impurities** to form the second region using the **gate electrode** as mask; (c) forming a sidewall (16a) on each side of each **gate electrode**; (d) introducing **n type** impurities to form the first region, using the **gate electrode** and sidewalls as mask; (e) introducing **p type** impurities to form the **source/drain region**

of the p channel MISFET using the **gate electrode** and sidewalls as mask.

ADVANTAGE - The CMOS device has good threshold voltage versus channel length characteristics. The method allows the effective channel length to be increased even if gate length is reduced by increasing the sidewall thickness and allowing the impurity contg. regions to reach positions close to both ends of the **gate electrode**.

1f

Abstract (Equivalent): EP 166167 B

A process for fabricating a **semiconductor device** having p-channel and n-channel ISFETs, a first one of which is formed at a first surface region (3) that has a first type of conductivity in a **semiconductor substrate** (1) and a second one of which is formed in a second surface region (2) of a second type of conductivity formed in said **semiconductor substrate** (1), comprising: (a) forming a **gate electrode** (8) for each of said MISFET on a **gate insulating film** (5), said **gate electrode** (8) having two sides: (b) forming first sub regions (15) by introducing **n-type** impurities into a region in which an n-channel MISFET is to be formed, using said **gate electrode** as a mask; (c) forming a sidewall (16a) on each side of each **gate electrode** (8) by depositing an **insulating film** (16) on the whole surface of said **semiconductor substrate** (1) and etching the whole surface thereof by reactive ion etching; (d) forming second sub regions (18) by introducing **n-type** impurities into the region in which said n-channel MISFET is to be formed, using said **gate electrode** (8) and said sidewalls (16a) as masks, said second sub regions (18) being deeper than said first sub regions (15) and having a **higher impurity concentration** than said first sub regions (15), and said second sub regions (18) together with said first sub regions (15) forming **source and drain regions** (19,20) of said n-channel MISFET; and (e) forming third sub regions (22) by introducing **p-type** imourities into a region in which a p-channel MISFET is to be formed, using said **gate electrode** (8) and said sidewalls (16a) as masks, said third sub regions (22) forming the **source and drain regions** (23,24) of said p-channel MISFET. (9pp)

Abstract (Equivalent): US 4891326 A

Semiconductor device is mfd. with n-channel MISFETS having **source and drain regions**, each of LDD construction, and p-channel MISFETS with **source and drain regions** each of a single region, formed in a 1st **semiconductor region** having **p-type** conductivity, and in a 2nd **semiconductor region** having **n-type** conductivity, respectively, in a **semiconductor substrate**. A **gate electrode** is formed for each of the n-channel MISFETS and p-channel MISFETS. Each **gate electrode** has two sides, and for each n-channel MISFET is formed over 1st **semiconductor region** in the **substrate**. The **gate electrode** for each p-channel MISFET is formed over 2nd **semiconductor region** in the **substrate**. First regions are formed by introducing **n-type** impurities into 1st **semiconductor region**, in which n-channel MISFETS will be formed, using **gate**

electrodes as masks. A sidewall insulator is formed on each sides of the **gate electrodes** of the n-channel MISFETS and the p-channel MISFETS. Second **regions** are formed by introducing **n-type** impurities into 1st **semiconductor region**, in which **n-channel** MISFETS will be formed, using **gate electrodes** and the sidewall insulators as masks to form 2nd regions at both sides of each **gate electrode** for the **n-channel** MISFETS. The 2nd **regions**, deeper than 1st regions, have a higher impurity concn. than the first regions. The 2nd regions form a **source region** and a **drain region** of the **n-channel** MISFETS together with 1st regions. The 1st regions and 2nd regions form LDD construction. Finally, third single **p-type** regions are formed by introducing **p-type** impurities into 2nd **semiconductor region**, in which **p-channel** MISFETS will be formed, using **gate electrodes** and sidewall **insulators** as masks, to form third single **p-type** regions at both sides of each **gate electrode** for **p-channel** MISFETS. The third **regions** are formed so its ends are located under the **gate electrode**. (7pp)

09/12/2002 09/837,397

58/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004339390

WPI Acc No: 1985-166268/198528

Related WPI Acc No: 1986-205989

Semiconductor module with two intercoupled circuits - which are on same semiconductor substrate, both of MOS FET type with different drain structures

Patent Assignee: HITACHI LTD (HITA)

Inventor: ISHIHARA M; IWAI H; MATSUMOTO T; MITSUSADA K; MIYAZAWA K; KATTO H ; OKUYAMA K

Number of Countries: 007 Number of Patents: 018

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3446928	A	19850704	DE 3446928	A	19841221	198528	B
GB 2152284	A	19850731	GB 8432417	A	19841221	198531	
JP 60136374	A	19850719	JP 83243801	A	19831226	198535	
FR 2561042	A	19850913				198543	
GB 2186426	A	19870812	GB 872881	A	19870209	198732	
GB 2152284	B	19880106				198801	
GB 2186426	B	19880106				198801	
IT 1179545	B	19870916				199036	
JP 3248470	A	19911106				199151	
US 5276346	A	19940104	US 84686598	A	19841226	199402	
			US 86825587	A	19860203		
			US 86937452	A	19861201		
			US 87106341	A	19871009		
			US 88198597	A	19880523		
			US 89390424	A	19890804		
			US 89404618	A	19890908		
			US 92815863	A	19920102		
KR 9301563	B1	19930304	KR 848171	A	19841220	199418	
			KR 9218775	A	19921013		
KR 9301564	B1	19930304	KR 848171	A	19841220	199418	
KR 9306139	B1	19930707	KR 848171	A	19841220	199426	
			KR 9218776	A	19921013		
US 5436483	A	19950725	US 84686598	A	19841226	199535	
			US 86825587	A	19860203		
			US 86937452	A	19861201		
			US 87106341	A	19871009		
			US 88198597	A	19880523		
			US 89390424	A	19890804		
			US 89404618	A	19890908		
			US 92815863	A	19920102		
			US 93142965	A	19931029		
US 5436484	A	19950725	US 84686598	A	19841226	199535	
			US 86825587	A	19860203		
			US 86937452	A	19861201		
			US 87106341	A	19871009		
			US 88198597	A	19880523		
			US 89390424	A	19890804		

09/12/2002 09/837, 397

			US 89404618	A 19890908
			US 92815863	A 19920102
			US 93143151	A 19931029
US 5534723	A	19960709	US 84686598	A 19841226 199633
			US 86825587	A 19860203
			US 86937452	A 19861201
			US 87106341	A 19871009
			US 88198597	A 19880523
			US 89390424	A 19890804
			US 89404618	A 19890908
			US 92815863	A 19920102
			US 93142965	A 19931029
			US 95431568	A 19950427
US 5610089	A	19970311	US 84686598	A 19841226 199716
			US 86825587	A 19860203
			US 86937452	A 19861201
			US 87106341	A 19871009
			US 88198597	A 19880523
			US 89390427	A 19890804
			US 89404618	A 19890908
			US 92815863	A 19920102
			US 93142965	A 19931029
			US 95429868	A 19950427
DE 3448619	A1	19980219	DE 3446928	A 19841221 199813
			DE 3448619	A 19841221

Priority Applications (No Type Date): JP 83243801 A 19831226; JP 90406691 A 19900000; JP 8516508 A 19850201

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3446928	A		26		Cont of application US 84686598
US 5276346	A		23	H01L-029/06	Div ex application US 86825587
					Cont of application US 86937452
					CIP of application US 87106341
					Cont of application US 88198597
					CIP of application US 89390424
					Cont of application US 89404618
					Div ex patent US 4717684
KR 9301563	B1			H01L-029/78	Div ex application KR 848171
KR 9306139	B1			H01L-029/78	Div ex application KR 848171
US 5436483	A		23	H01L-029/06	Cont of application US 84686598
					Div ex application US 86825587
					Cont of application US 86937452
					CIP of application US 87106341
					Cont of application US 88198597
					CIP of application US 89390424
					Cont of application US 89404618
					Cont of application US 92815863
					Div ex patent US 4717684
					Cont of patent US 5276346
US 5436484	A		24	H01L-029/06	Cont of application US 84686598
					Div ex application US 86825587
					Cont of application US 86937452

			CIP of application US 87106341
			Cont of application US 88198597
			CIP of application US 89390424
			Cont of application US 89404618
			Cont of application US 92815863
			Div ex patent US 4717684
			Cont of patent US 5276346
US 5534723	A	22 H01L-029/06	Cont of application US 84686598
			Div ex application US 86825587
			Cont of application US 86937452
			CIP of application US 87106341
			Cont of application US 88198597
			CIP of application US 89390424
			Cont of application US 89404618
			Cont of application US 92815863
			Div ex application US 93142965
			Div ex patent US 4717684
			Cont of patent US 5276346
			Div ex patent US 5436483
US 5610089	A	25 H01L-021/8238	Cont of application US 84686598
			Div ex application US 86825587
			Cont of application US 86937452
			CIP of application US 87106341
			Cont of application US 88198597
			CIP of application US 89390427
			Cont of application US 89404618
			Cont of application US 92815863
			Div ex application US 93142965
			Div ex patent US 4717684
			Cont of patent US 5276346
			Div ex patent US 5436483
DE 3448619	A1	H01L-023/60	Div ex application DE 3446928
KR 9301564	B1	H01L-029/784	Div ex patent DE 3446928

Abstract (Basic): DE 3446928 A

A first circuit comprises at least one MIS element and is coupled to a second circuit. The two circuits are formed on a common **semiconductor substrate** (20). The first circuit comprises a double diffused **drain** structure using phosphor to produce lightly doped **N-type** region while the second circuit using arsenic to produce heavily doped **N-type** region has a simple diffused **drain** structure. Pref. the first circuit is an inner one, while the second circuit is of an electrostatic protection type.

The second circuit protects the first one against abnormal external signals. The second circuit has diffused resistors (31) and clamping MIS elements. The resistor may have a simple diffused **drain** structure. The module may have an input terminal spot, and the resistor may be connected to the internal first circuit and to this spot.

USE - For miniature integrated circuits with MOS FETs and high integrating density.

Dwg.7/19

Abstract (Equivalent): GB 2152284 B

A **semiconductor** integrated circuit device, formed in a major surface of a **semiconductor substrate**, having at least one MISFET for a first circuit, the at least one MISFET having a diffused **drain region**, each **drain region** of the at least one MISFET comprising a first **doped** region of **high concentration** and a second **doped** region of relatively low **concentration** of the same conductivity type as the first doped region, the first doped region being within the second doped region, wherein a protective element of a second circuit electrically connected to the first circuit, for protecting the one MISFET from an external surge **voltage** introduced through an external terminal, has a **doped** region of a **high concentration** substantially the same as the first doped region and of the same conductivity type and no region having a concentration and conductivity type substantially the same as the second doped region and which is in contact with the region of **high concentration** of the protective element, wherein the region of **high concentration** of the protective element is formed simultaneously with the first doped region.

GB2186426 A **semiconductor** integrated circuit device, formed in a major surface of a **semiconductor substrate**, having at least one MISFET for a first circuit, the at least one MISFET having a diffused **drain region**, and a **gate electrode** with side wall **spacers** on either side of the **gate electrode**, each **drain region** of the at least one MISFET comprising a first **doped** region of **high concentration** and a second **doped** region of relatively low **concentration** of the same conductivity type as the first doped region, and in contact with the first doped region, wherein a protective element of a second circuit electrically connected to the first circuit for protecting the first circuit from an external surge **voltage** introduced through an external terminal, has a **doped** region of a **high concentration** substantially the same as the first doped region and of the same conductivity type and no region having a concentration and conductivity type substantially the same as the second doped region and which is in contact with the region of **high concentration** of the protective element, wherein the region of **high concentration** of the protective element is formed simultaneously with the first doped region, and wherein the second doped region is formed in self-alignment with the **gate electrode**, and the first doped region is formed in self-alignment with one of the side wall **spacers** and the **gate electrode**.

Abstract (Equivalent): US 5610089 A

A method of manufacturing a **semiconductor** integrated circuit device, comprising the steps of:

providing a **semiconductor substrate** having a second MISFET forming region and an internal circuit forming region, with a first **gate insulating film** on said second MISFET forming region, and a first **gate electrode** of a second MISFET on said first **gate insulating film**, and with a second **gate insulating film** on said internal circuit forming region, and a second **gate electrode** of a first MISFET on said second **gate insulating film**;

introducing into said second MISFET forming region at least one impurity in self-alignment with said first **gate electrode** to form respectively at least a first **semiconductor** region of a first conductivity type such that a pn-junction is formed, under said first **gate electrode**, between said first **semiconductor** region and said **semiconductor substrate** ;

introducing into said internal circuit forming region an impurity in self-alignment with said second **gate electrode** to form a second **semiconductor** region of said first conductivity type such that a pn-junction is formed, under said second **gate electrode**, between said second **semiconductor** region and said **semiconductor substrate** and such that an **impurity concentration** of said first **semiconductor** region is higher than that of said second **semiconductor** region;

forming a third **semiconductor** region of said first conductivity type in said internal circuit forming region by introducing an impurity in said internal circuit forming region; and

forming a first bonding pad, on said **semiconductor substrate**, being electrically connected to said first **semiconductor** region,

said second **semiconductor** region being formed between said third **semiconductor region** and a **channel** forming region of said first MISFET,

an **impurity concentration** of said third **semiconductor** region being higher than that of said second **semiconductor** region,

said second and third **semiconductor regions** serving as a **drain region** of said first MISFET, and

said first **semiconductor region** serving as a **drain region** of said second MISFET.

Dwg.18/27

US 5534723 A

A **semiconductor** integrated circuit device, comprising:
an output pad formed on a **semiconductor substrate**;
a first output MISFET having a first **gate insulating film** on said **semiconductor substrate** and a first **gate electrode**, with opposed edges, on said first **gate insulating film**, and further having **source** and **drain regions** and a first **channel forming region** in said **semiconductor substrate**; and

a first MISFET having a second **gate insulating film** on said **semiconductor substrate** and a second **gate electrode**, with opposed edges, on said second **gate insulating film**, and further having **source** and **drain regions** and a second **channel forming region** in said **semiconductor substrate**,

said **drain region** of said first MISFET including a first doped subregion of relatively **high impurity concentration** and a second doped subregion of relatively **low impurity concentration**,

said second doped subregion being formed between said first doped subregion and said second **channel forming region**,

said **source** and **drain regions** of said first

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MISFET being of a same conductivity type as said **source** and
drain regions of said first output MISFET,
said first MISFET being included in an internal circuit of the
semiconductor integrated circuit device,
said **source region** of said first output MISFET being
electrically connected to a ground potential, and
said **drain region** of said first output MISFET being
electrically connected to said output pad,
wherein a backward breakdown **voltage** at a pn-junction between
said **semiconductor substrate** and said **drain**
region of said first output MISFET at a **drain** edge thereof
is lower than a backward breakdown **voltage** at a pn-junction
between said **semiconductor substrate** and said **drain**
region of said first MISFET at a **drain** edge thereof.

Dwg. 9/27

58/3,AB/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
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04854805

FIELD EFFECT TRANSISTOR AND ITS DRIVING METHOD AND INVERTER, LOGIC CIRCUIT
AND SRAM USING IT

PUB. NO.: 07-147405 [JP 7147405 A]
PUBLISHED: June 06, 1995 (19950606)
INVENTOR(s): IMAI KIYOTAKA
APPLICANT(s): NKK CORP [000412] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 06-096077 [JP 9496077]
FILED: May 10, 1994 (19940510)

ABSTRACT

PURPOSE: To provide a field effect transistor which can ensure a noise margin in stability and low-voltage operation without increasing the chip size of an inverter, a logic circuit, an SRAM and the like.

CONSTITUTION: This is a field effect transistor composed of a single layer and a multilayer gate electrode. For instance, a gate insulating film 6 is formed in the surface of a channel region of a p-type semiconductor substrate 1 in which an n-type source-drain region is formed, and an n-type conductive layer in which the p-type impurities of low concentration are doped is formed on the gate oxide film 6. In the field effect transistor, when a voltage is applied between a gate and a source in such a direction that the transistor is turned on, a depletion layer generated in the gate electrode 9 is dynamically varied to change a virtual gate oxide film, thereby positively changing the electrical characteristic of a field effect transistor.

58/3,AB/12 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO
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03620768

SEMICONDUCTOR INTEGRATED CIRCUIT

PUB. NO.: 03-283668 [JP 3283668 A]
PUBLISHED: December 13, 1991 (19911213)

INVENTOR(s): NAMETAKE MASATAKE
KOBAYASHI YUTAKA
HIRAISHI ATSUSHI
AKIOKA TAKASHI
YOKOYAMA YUJI
IWAMURA MASAHIRO
TAKAHASHI SHIGERU
UCHIDA HIDEAKI
IDE AKIRA

APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)

APPL. NO.: 02-084503 [JP 9084503]
FILED: March 30, 1990 (19900330)

JOURNAL: Section: E, Section No. 1179, Vol. 16, No. 108, Pg. 103,
March 17, 1992 (19920317)

ABSTRACT

PURPOSE: To protect a switching element even when static electricity is impressed on a terminal of a **semiconductor** integrated circuit and thereby to prevent a damage of the integrated circuit by providing the switching element with a means of protection from electrostatic breakdown.

CONSTITUTION: A P well region 6 is formed on a P⁻ type **semiconductor substrate** 1 and a field **insulation** film 8 is formed. Element isolation is made by this **insulation** film 8 and a **channel stopper region**. Next, a **gate insulation** film 16 is formed and a **gate electrode** 17 is formed in the prescribed upper part thereof. High-concentration **impurity** regions 9 (n⁺) of a **drain** and a **source** are formed by doping an **n-type** impurity (P or As) before a side wall spacer 18 is formed, or by doping such an **n-type** impurity as P having a high diffusion coefficient after the side wall spacer 18 is formed. By impressing a supply **voltage** on an **n-type semiconductor** region 7, besides, a charge is neutralized in the region 7 even when a negative potential is impressed on the **drain**.

58/3,AB/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO
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03160282

SEMICONDUCTOR NONVOLATILE MEMORY

PUB. NO.: 02-135782 [JP 2135782 A]
PUBLISHED: May 24, 1990 (19900524)
INVENTOR(s): KOJIMA YOSHIKAZU
APPLICANT(s): SEIKO INSTR INC [000232] (A Japanese Company or Corporation),
JP (Japan)
APPL. NO.: 63-290547 [JP 88290547]
FILED: November 17, 1988 (19881117)
JOURNAL: Section: E, Section No. 964, Vol. 14, No. 374, Pg. 37, August
13, 1990 (19900813)

ABSTRACT

PURPOSE: To operate at a low **voltage** by providing an opposite conductivity type second **semiconductor** region to a first conductivity type of a first conductivity type **semiconductor substrate** inside the first **semiconductor** region having higher concentration than that of the **substrate**.

CONSTITUTION: A region 9 is doped with low concentration **N-type impurity** inside a higher concentration **impurity** region 8 than that of a **P-type** silicon substrate 1, a floating **gate electrode** 5 is provided on the surfaces of the regions 8 and 9 through a gate oxide film 4, and a control **gate electrode** 7 is further formed on the **electrode** 5 through a control **gate insulating film**

6. **N^{sup +}** type **source** and **drain regions** 2, 3 are provided at an interval on the **substrate** under the **electrode** 5. Thus, since the **impurity concentration** of the surface of a **channel region** is reduced in the region 9 to decrease the threshold value **voltage** after it is irradiated with an ultraviolet ray, it can be easily operated in a low **voltage** range while satisfying programming characteristics and isolating characteristics.

58/3,AB/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO
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03119071

SEMICONDUCTOR DEVICE

PUB. NO.: 02-094571 [JP 2094571 A]
PUBLISHED: April 05, 1990 (19900405)
INVENTOR(s): YOSHIMI MAKOTO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-246405 [JP 88246405]
FILED: September 30, 1988 (19880930)
JOURNAL: Section: E, Section No. 944, Vol. 14, No. 292, Pg. 92, June
25, 1990 (19900625)

ABSTRACT

PURPOSE: To obtain a **semiconductor device** having a composite transmitting function with one transistor by forming the part of an **insulating film** of a thin ferrodielectric film in which its polarizing direction is varied between **high concentration impurity** regions, and forming the polarization of the thin film by an electric field distribution due to pentode operation.

CONSTITUTION: A **semiconductor device** is composed of a **gate electrode** 4 made of a tungsten film W formed on the surface of a **P-type** silicon **substrate** 1 having approximately $1 \times 10^{16} \text{ cm}^{-3}$ of **impurity concentration** through a zircon lead titanate 3 as a **gate insulating film** 3, and **source, drain regions** 2A, 2B made of **N-type** impurity regions. One of the regions 2A, 2B of this device is used as an input terminal (source) 2A, the other is used as an output terminal (**drain**) 2B, 0, 5 and 3 V are respectively applied to the terminals 2A, 2B and the gate 4 to be operated as a pentode operation. Then, the polarization of the ferrodielectric element can be freely altered by varying the **voltages** to be applied to the terminals. Unidirectional transmitting characteristic or bidirectional characteristic can be also provided.

58/3,AB/15 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO
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03115067

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 02-090567 [JP 2090567 A]
PUBLISHED: March 30, 1990 (19900330)
INVENTOR(s): IZAWA RYUICHI
TAKEDA EIJI
IGURA YASUO
YADORI SHOJI
KURE TOKUO
HISAMOTO MASARU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-240987 [JP 88240987]
FILED: September 28, 1988 (19880928)
JOURNAL: Section: E, Section No. 942, Vol. 14, No. 282, Pg. 110, June
19, 1990 (19900619)

ABSTRACT

PURPOSE: To obtain a fine MIS transistor which is high in breakdown strength, Gm characteristic, and punch-through resistance by a method wherein the base of a **gate electrode** is provided inside a **substrate**, a **low concentration source.drain** is provided so as to prevent a **gate electrode** from overlapping directly with a **high concentrated source.drain**.

CONSTITUTION: A **gate electrode** 5 is formed inside the groove provided to a Si **substrate** 1 doped with **P-type** or **n-type impurity**. A **low concentration source.drain** 2 is provided to the sides of the groove sandwiching the groove in between them, a **high concentration source.drain** 7 is formed on both the sides of the **low concentration source.drain** 2s being in contact with them, and a **source.drain** region is doped with impurity whose conductivity type is opposite to that of the **substrate** 1. And, the **gate electrode** 5 and the **substrate** 1 are isolated from each other by a **gate insulating layer** 3. A channel injecting layer 4 controlling V_{th} (threshold voltage) is formed on the base of the groove in which the **gate electrode** has been formed. An **insulating film** 6 is formed on the side wall of the **gate electrode** 5 to enable an ion-implanting end at the formation of the **high concentration source.drain** 7 to be separate from the **gate electrode** 5.

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58/3,AB/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO
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03009668

MIS TYPE TRANSISTOR

PUB. NO.: 01-307268 [JP 1307268 A]
PUBLISHED: December 12, 1989 (19891212)
INVENTOR(s): AOKI TAKAHIRO
TOMIZAWA MASAAKI
YOSHII AKIRA
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese
Company or Corporation), JP (Japan)
APPL. NO.: 63-138884 [JP 88138884]
FILED: June 06, 1988 (19880606)
JOURNAL: Section: E, Section No. 895, Vol. 14, No. 105, Pg. 99,
February 26, 1990 (19900226)

ABSTRACT

PURPOSE: To obtain a normally-off MISFET having no kink characteristic and high Gm (mobility) by bringing the surface to **low concentration** and the base to **high concentration** in the **impurity concentration** distribution of a thin-film SOI **substrate**.
CONSTITUTION: **Source-drain regions** 15, 16 are formed to the surface of a single crystal silicon layer (an SOI **substrate**) 12, and an N^(sup +) polysilicon **gate electrode** 18 is shaped onto a **channel region** between these **source-drain regions** 15, 16 through a **gate insulating film** 17. **Impurity concentration** distribution just under a channel is set so that threshold **voltage** is brought to the state of normally-off and kind characteristics are not acquired. The thickness of an **insulator film** 11 is brought to a value not affected by an SOI channel, and the thickness of 30nm of the surface of the SOI **substrate** 12 is brought to a **P type** and **impurity concentration** of 10^(sup 15)cm^(sup -3) and the thickness of 20nm of the base of the SOI **substrate** 12 to the **P type** and **impurity concentration** of 2X10^(sup 17)cm^(sup -3), thus controlling threshold **voltage** to a normally-off type. Accordingly, the normally-off of high Gm can be realized.

58/3,AB/17 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO
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02505274

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 63-122174 [JP 63122174 A]
PUBLISHED: May 26, 1988 (19880526)
INVENTOR(s): IZAWA RYUICHI
TAKEDA EIJI
IGURA YASUO
HAMADA AKIYOSHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 61-266543 [JP 86266543]
FILED: November 11, 1986 (19861111)
JOURNAL: Section: E, Section No. 665, Vol. 12, No. 369, Pg. 139,
October 04, 1988 (19881004)

ABSTRACT

PURPOSE: To relax an electric field spreading in the transverse direction between a **source** and a **drain**, to suppress the occurrence of an avalanche breakdown and a hot carrier, and to realize a hig-withstand-voltage and a high-speed operation by a method wherein a region coming into contact with a **gate insulating film**, out of a depleted **region** in a **source-drain region**, is covered with a **gate electrode**.

CONSTITUTION: An **n-type low-concentration source-drain region** 3 is formed by introducing an **n**-type impurity into a **p-type Si substrate** 8 and by self-aligning with a first **gate electrode** 1 by making use of the first **gate electrode** 1 and an **insulating film** 5 as a mask. Then, an electric-conductive film composed of polycrystalline silicon, a silicide or the like, doped with an electric-conductive impurity of high concentration is deposited on the whole surface. After that, said electric-conductive film is etched anisotropically so that a second **gate electrode** 6 remains only at the side wall of the first **gate electrode** 1. Then, after the **insulating film** has been deposited again on the whole surface, an etching process is executed so that an **insulating film** 7 can be formed at the side wall so as to cover the second **gate electrode** 6. Tie film overlaps with the **low-concentration source-drain region** 3 by means of the second **gate electrode** 6. The overlapping amount can be controlled by the deposited film thickness for the second **gate electrode** 6 and by the overetching amount of said electric-conductive film.

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58/3,AB/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO
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01973176

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

PUB. NO.: 61-187276 [JP 61187276 A]
PUBLISHED: August 20, 1986 (19860820)
INVENTOR(s): TANAKA KENICHI
ISHIHARA HIROSHI
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-028102 [JP 8528102]
FILED: February 14, 1985 (19850214)
JOURNAL: Section: E, Section No. 470, Vol. 11, No. 11, Pg. 153,
January 13, 1987 (19870113)

ABSTRACT

PURPOSE: To make the titled device to correspond to **voltage** applied on rewriting work rapidly, and to hold written contents stably by interposing an **insulating film** displaying current characteristics depending upon the direction of applied **voltage** between a floating gate and a **drain high-concentration impurity region**.

CONSTITUTION: A LOCOS region 29 and a protective film 21 are formed to a **P-type** silicon **substrate** 20, an opening is bored to one part of the protective film 21 and a thin oxide film 22 is shaped through thermal oxidation, and an impurity is introduced to an oxide film 22 section while using a resist 28 as a mask. The concentration distribution of the **impurity** in the thin **insulating film** 22 is increased with an approach to an N^(sup +) region 23 formed to the surface of the **semiconductor substrate** and made the highest in a section brought into contact with the N^(sup +) region 23 by selecting energy on the implantation of ions within the extent of a projection range at that time. A floating **gate** 24, an **insulating film** 25, a control **gate** 26, a **gate electrode** 27, N^(sup +) regions 23a-23c as a **source** or a **drain**, Al wirings, etc. are shaped. Accordingly, memory contents can be rewritten at low **voltage**, and written contents can be held stably.

58/3,AB/21 (Item 21 from file: 347)
DIALOG(R) File 347:JAPIO
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01701668

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-180168 [JP 60180168 A]
PUBLISHED: September 13, 1985 (19850913)
INVENTOR(s): TAKI MASUYUKI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 59-035160 [JP 8435160]
FILED: February 28, 1984 (19840228)
JOURNAL: Section: E, Section No. 376, Vol. 10, No. 20, Pg. 48, January
25, 1986 (19860125)

ABSTRACT

PURPOSE: To obtain high field inversion **voltage** by a simple process by forming a **gate electrode**, shaping an organic resin layer on the whole surface and forming a **high-concentration impurity** diffusion layer while leaving the organic resin layer on a gate side-wall by utilizing the anisotropy of reactive ion etching.

CONSTITUTION: A gate 34 consisting of a polycrystalline silicon film is formed on a **P type** silicon **semiconductor substrate** 32 with a field oxide film 31 through a thin **gate insulating film** 33, and **low-concentration impurity** layers 35 are shaped to **source** and **drain regions** by implanting **N type** ions while using the gate 34 as a mask. An organic resin layer 36 is formed by applying an organic resin, and organic resin film patterns 36a are left so as to cover only the side surface of the gate 34 and sections in the vicinity of the side surface through anisotropic reactive ion etching to the whole surface of the organic resin layer 36. **N type** ions are implanted while using the resin films 36a and the gate 34 as masks to form **high-concentration impurity** layers 37.

58/3,AB/22 (Item 22 from file: 347)
DIALOG(R)File 347:JAPIO
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01655969

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-134469 [JP 60134469 A]
PUBLISHED: July 17, 1985 (19850717)
INVENTOR(s): YOSHIKAWA KUNIYOSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 58-242601 [JP 83242601]
FILED: December 22, 1983 (19831222)
JOURNAL: Section: E, Section No. 360, Vol. 09, No. 295, Pg. 60,
November 21, 1985 (19851121)

ABSTRACT

PURPOSE: To reduce ion implantation processes, and to simplify processes by forming a film containing an impurity to the surface of a **substrate** and diffusing the impurity into the film through heat treatment under predetermined conditions when an MOS transistor with a **drain** region in low impurity concentration is prepared.

CONSTITUTION: A thick field oxide film 12 is formed to the peripheral section of a P type Si **substrate** 11, a thin oxide film 13 is applied on the surface of the **substrate** 11 surrounded by the oxide film 12, and B ions for controlling threshold **voltage** are implanted to the surface layer of the **substrate** 11 through the oxide film 13. A **gate electrode** 15 is formed at the central section of the surface of the **substrate** 11 through a **gate insulating** film 16 consisting of the film 13, and an SiO₂ film 17 containing a P impurity is applied on the whole surface. The impurity in the film 17 is diffused through heat treatment for 20min at 900°C in N₂ gas to form N⁻ type regions 18 and 19 to the surface layer section of the **substrate** 11 on both sides of the **electrode** 15. The films 17 are left only on both side surfaces of the **electrode** 15 as 17', and As ions are implanted to the regions 18 and 19 again to form N⁺ type **source** and **drain regions** 20, 21 connected to the regions 18 and 19.

58/3,AB/23 (Item 23 from file: 347)
DIALOG(R) File 347:JAPIO
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01595978

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-074478 [JP 60074478 A]
PUBLISHED: April 26, 1985 (19850426)
INVENTOR(s): NAKADA YOSHIRO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company
or Corporation), JP (Japan)
APPL. NO.: 58-182144 [JP 83182144]
FILED: September 29, 1983 (19830929)
JOURNAL: Section: E, Section No. 339, Vol. 09, No. 212, Pg. 38, August
29, 1985 (19850829)

ABSTRACT

PURPOSE: To form a region with excellent controllability, less dispersion at **low impurity concentration** by a method wherein dual diffusion in **drain, source regions** of MOSFET is performed by oxidation of poly Si gate.

CONSTITUTION: A thermal oxide film 2 to be a **gate insulating film** for controlling threshold value **voltage** is formed on a **P type substrate** 1 and poly crystalline Si is deposited on the film 2 to form a **gate electrode** 3. The **source, drain regions** 6 are implanted with As^(sup +) ion at **high concentration** utilizing the **gate electrode** 3 as a mask. Firstly the surface of poli Si is oxidized to form an oxide film 7. Secondly the film 7 is removed to narrow the width. Finally the other regions 8 at **low impurity concentration** are formed utilizing the **gate electrodes** 3 as a mask to be LDD structure.

58/3, AB/24 (Item 24 from file: 347)
DIALOG(R) File 347: JAPIO
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01113377

INSULATING GATE TYPE FIELD EFFECT SEMICONDUCTOR
DEVICE

PUB. NO.: 58-050777 [JP 58050777 A]
PUBLISHED: March 25, 1983 (19830325)
INVENTOR(s): MEGURO SATOSHI
SUZUKI NORIO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 56-147909 [JP 81147909]
FILED: September 21, 1981 (19810921)
JOURNAL: Section: E, Section No. 181, Vol. 07, No. 136, Pg. 38, June
14, 1983 (19830614)

ABSTRACT

PURPOSE: To contrive the high withstand **voltage** of a finely formed MISFET and enable the easy manufacture of an off set gate structure necessary to the high withstand voltage thereof with good accuracy, by forming **low impurity concentration** regions by utilizing the mask function of the **gate electrode** itself, and constituting so that **high impurity concentration** regions are formed with the **insulating film** thickness provided on the surface of the **gate electrode** as a mask.

CONSTITUTION: In the off set gate structure of an MISFET, **low concentration N type regions** 18, 19 of **source** and **drain regions** are formed by the mask function of a **gate electrode** 12 itself on the sides thereof, and, by utilizing the sufficient difference of film thicknesses between an SiO₂ film 21 due to a thermal oxidation and a CVD on the surface of the **gate electrode** 12 and an SiO₂ film 22 on a substrate 1, **high concentration N⁺** type regions 26, 27 are formed at the position off the **gate electrode** on the further outside with the former SiO₂ film 21 as a mask. Therefore, since self-align systems is all performed not by using said over etching but by using particularly the difference of an SiO film to form an off set gate structure, the off set gate can be easily obtained with good accuracy.

58/3,AB/19 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO
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02084376

MOS TYPE SEMICONDUCTOR DEVICE

PUB. NO.: 62-001276 [JP 62001276 A]
PUBLISHED: January 07, 1987 (19870107)
INVENTOR(s): KIYONO JUNJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-139570 [JP 85139570]
FILED: June 26, 1985 (19850626)
JOURNAL: Section: E, Section No. 511, Vol. 11, No. 169, Pg. 7, May 30,
1987 (19870530)

ABSTRACT

PURPOSE: To speed up operation, to increase withstanding **voltage** and to fine an element by forming **source-drain regions** by utilizing a **gate electrode** and shallowing junction depth and lowering **impurity concentration** at the **lower** position of a projecting section in a second **electrode layer**.

CONSTITUTION: An insulating isolation region 12 is formed onto a P-type silicon **substrate** 11, a **gate insulating film** 13 is shaped in an element region by a thin silicon oxide film, a polysilicon layer 14 is applied onto the **insulating film** 13, resistance is lowered, and a molybdenum silicide layer 15 is superposed and applied onto the layer 14. The molybdenum silicide layer 15 and the polysilicon layer 14 are etched while using a resist layer 16 shaped according to a pattern so as to be made longer than gate length as a mask. A **gate electrode** 17 is formed by a first **electrode layer** 14a and a second **electrode layer** 15a, and both ends of the second **electrode layer** 15a are projected to both sides from the first **electrode layer** 14a. The resist layer 16 is removed, arsenic ions are implanted, and a **source region** 18 and a **drain region** 19 are shaped through a self-alignment manner.

61/3,AB/1 (Item 1 from file: 347)
DIALOG(R) File 347:JAPIO
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03129969

MIS TYPE SEMICONDUCTOR DEVICE

PUB. NO.: 02-105469 [JP 2105469 A]
PUBLISHED: April 18, 1990 (19900418)
INVENTOR(s): NOGUCHI KOU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-258618 [JP 88258618]
FILED: October 13, 1988 (19881013)
JOURNAL: Section: E, Section No. 949, Vol. 14, No. 316, Pg. 149, July
06, 1990 (19900706)

ABSTRACT

PURPOSE: To reduce a channel length without increasing a junction capacity between an impurity diffusion layer and a substrate by containing one conductivity type diffusion layer whose impurity concentration is lower than that of a semiconductor substrate which is in contact with a bottom side of a source/drain region consisting of a reverse conductivity type diffusion layer in contact with an edge end section of a gate insulating film and is formed apart from a channel region.

CONSTITUTION: A semiconductor device contains; a p-type silicon substrate 1, a gate insulating film 2 and a polycrystalline silicon gate electrode 3, an N-type low concentration diffusion layer 4 of a source/drain region having an impurity concentration of about 5×10^{17} (10^{18}) cm⁻³, for example, which is formed in an area near a channel region to come into contact with an edge end section of the gate insulating film 2, an N-type high concentration diffusion layer 5 of a source/drain region having an impurity concentration of about 1×10^{20} cm⁻³, for example, which is in contact with an end side of an N-type low concentration diffusion layer 4 and formed apart from a channel region, and a P-type low concentration diffusion layer 7 of an impurity concentration of about 5×10^5 cm⁻³ which is in contact with a bottom side of the N-type high concentration diffusion layer 5 and is formed inside the p-type silicon substrate 1 apart from a channel region further than the N-type high concentration diffusion layer 5.

61/3,AB/2 (Item 2 from file: 347)
DIALOG(R) File 347:JAPIO
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01593771

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-072271 [JP 60072271 A]
PUBLISHED: April 24, 1985 (19850424)
INVENTOR(s): WADA TETSUNORI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 58-178130 [JP 83178130]
FILED: September 28, 1983 (19830928)
JOURNAL: Section: E, Section No. 338, Vol. 09, No. 208, Pg. 89, August
24, 1985 (19850824)

ABSTRACT

PURPOSE: To enable the formation of the objective impurity distribution by self-alignment by a method an impurity of the same conductivity type as that of a **substrate** is selectively introduced in such a manner that part of the impurity in the neighborhood of the channel of the **source** and **drain regions** is cancelled.

CONSTITUTION: A **gate insulation film** 12 is formed on the **P type semiconductor substrate** 11, and a **gate electrode** 14 is formed with an oxidation resistant mask material 13 as a mask. The **source** and **drain regions** 15 and 16 are formed by introduction of an **N type** impurity in this state. Next, oxide films 17 are formed on the side walls of the **electrode** 14. Then, the surface of the **substrate** 11 is exposed by removal of the films 17 of the regions 15 and 16. In this state, the entire surface of the **substrated** is covered with an oxide film 18 containing an impurity of the **reverse conductivity** type to that of the **substrate**. When the film 18 is removed by the technique of reactive ion etching, films 18' containing the impurity of the **reverse conductivity** type to that of the **substrate** is left on the side walls of the **electrode**. The impurity in the film 18' is diffused into the **substrate**; thereby the impurity in the parts of the regions 15 and 16 in contact with the films 18' is cancelled, and accordingly regions 19 of a **low impurity concentration** are fo

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66/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014613993
WPI Acc No: 2002-434697/200246
XRAM Acc No: C02-123363
XRPX Acc No: N02-342196

Silicon carbide **semiconductor device** as metal-insulator-
semiconductor field-effect transistor, includes **P-type**
gate electrode and **N-type impurity** region
having **impurity concentration** which form buried **channel**
region

Patent Assignee: JAPAN SCI & TECHNOLOGY CORP (NISC-N); NAT INST ADVANCED
IND SCI & TECHNOLOGY (NAAD-N); DOKURITSU GYOSEI HOJIN SANGYO GIJUTSU SO
(DOKU-N); KAGAKU GIJUTSU SHINKO JIGYODAN (KAGA-N)

Inventor: ADACHI K; ARAI K; FUKUDA K; HARADA S; KOSUGI R; SENZAKI J

Number of Countries: 028 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020047125	A1	20020425	US 2001987271	A	20011114	200246 B
EP 1205981	A2	20020515	EP 2001309581	A	20011113	200246
JP 2002151680	A	20020524	JP 2000346455	A	20001114	200250

Priority Applications (No Type Date): JP 2000346455 A 20001114

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020047125	A1	14		H01L-031/312	
EP 1205981	A2	E		H01L-029/78	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI TR
JP 2002151680 A 9 H01L-029/78

Abstract (Basic): US 20020047125 A1

Abstract (Basic):

NOVELTY - A silicon carbide **semiconductor device**
includes a **P-type gate electrode** (8) formed on
a gate insulation layer, and an **N-type**
impurity region having an **impurity concentration** which form
a buried **channel region** (2) on a lower surface of the
gate insulation layer.

DETAILED DESCRIPTION - A silicon carbide (SiC) **semiconductor**
device comprises a **semiconductor substrate** (1) having
a **P-type SiC region**, a **gate insulation**
layer formed on the **SiC region**; a **P-type gate**
electrode formed on the **gate insulation layer**;
an **N-type impurity region** having an **impurity**
concentration to form a buried **channel region** on a
lower surface of the **gate insulation layer**; and
source and drain regions having **N-type**
impurity regions formed adjacent to the **gate insulation**
layer and **gate electrode**.

USE - As metal-insulator-**semiconductor** field-effect

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transistor on silicon carbide **substrate**.

ADVANTAGE - The SiC **semiconductor device** has increased channel mobility. The channel mobility is improved when optimizing the ratio between the **source/drain junction** depth and junction depth of the buried **channel region junction**. The surface orientation of the SiC **substrate** is optimized so that the device does not assume a normally on state. The device has high hot-carrier endurance and punch-through endurance.

DESCRIPTION OF DRAWING(S) - The figure depicts the fabrication of a metal-insulator-**semiconductor** field-effect transistor having a **P-type gate electrode** and buried **channel region**.

Semiconductor substrate (1)

Buried channel region (2)

P-type gate electrode (8)

pp; 14 DwgNo 1d/9

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66/3,AB/2 (Item 2 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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010782001
WPI Acc No: 1996-278954/199629
XRPX Acc No: N96-234570

P-type metal oxide semiconductor field effect transistor device suitable for CMOS technology - has gate electrode on upper surface of thin polysilicon layer having high impurity concentration of n-type ions and being formed in insulation layer above channel region doped with e.g. indium

Patent Assignee: AT & T CORP (AMTT); AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); LUCENT TECHNOLOGIES INC (LUCE)

Inventor: KIZILYLLI I C; KIZILYALLI I C

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19544945	A1	19960613	DE 1044945	A	19951201	199629	B
JP 8227992	A	19960903	JP 95335700	A	19951201	199645	
TW 304301	A	19970501	TW 95101220	A	19950211	199730	
CN 1132941	A	19961009	CN 95120272	A	19951127	199802	
US 5710055	A	19980120	US 94347980	A	19941201	199810	
			US 95478133	A	19950607		
US 5767557	A	19980616	US 94347980	A	19941201	199831	
			US 96656996	A	19960524		

Priority Applications (No Type Date): US 94347980 A 19941201; US 95478133 A 19950607; US 96656996 A 19960524

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19544945	A1	11		H01L-029/78	
JP 8227992	A	7		H01L-029/78	
US 5710055	A	9		H01L-021/265	Div ex application US 94347980
US 5767557	A			H01L-029/76	Cont of application US 94347980
TW 304301	A			H01L-027/105	
CN 1132941	A			H01L-029/78	

Abstract (Basic): DE 19544945 A

The semiconductor device includes an n-type substrate with a main surface upon which is located a channel region between p-type source and drain regions. The substrate contains an impurity ion from a group contg. Tm, Ga and their mixtures. On the channel region surface is formed a thin, insulating layer.

A first conductivity gate electrode is formed on the surface of the thin, insulating layer to act onto the channel region through the insulating layer.

The gate electrode contains polysilicon with a high impurity concentration of ions of the first conductivity. The semiconductor substrate is pref. a silicon.

USE/ADVANTAGE - For VLSI, ULSI. Sharp implanted doping

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profile and low diffusion of doping ions into substrate. Has improved short channel characteristics.

Dwg.1/10

Abstract (Equivalent): US 5710055 A

The semiconductor device includes an n-type substrate with a main surface upon which is located a channel region between p-type source and drain regions. The substrate contains an impurity ion from a group contg. Tm, Ga and their mixtures. On the channel region surface is formed a thin, insulating layer.

A first conductivity gate electrode is formed on the surface of the thin, insulating layer to act onto the channel region through the insulating layer.

The gate electrode contains polysilicon with a high impurity concentration of ions of the first conductivity. The semiconductor substrate is pref. a silicon.

USE/ADVANTAGE - For VLSI, ULSI. Sharp implanted doping profile and low diffusion of doping ions into substrate. Has improved short channel characteristics.

3,5,7/10

66/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010552116
WPI Acc No: 1996-049069/199605
Related WPI Acc No: 1995-267413
XRPX Acc No: N96-041166

Thin film **semiconductor** transistor device for e.g. printer driver - has crystalline **semiconductor** film with **low concentration doped regions** between **non-doped channel** and **high opposite conductivity doped drain** and **source regions** respectively

Patent Assignee: CASIO COMPUTER CO LTD (CASK)

Inventor: MIYAKAWA T; SHIMOMAKI S; WAKAI H

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5477073	A	19951219	US 94287849	A	19940809	199605 B
JP 7111333	A	19950425	JP 93342239	A	19931215	199605

Priority Applications (No Type Date): JP 93342239 A 19931215; JP 93226715 A 19930820; JP 93342109 A 19931214

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5477073	A	11	H01L-029/04	
JP 7111333	A	7	H01L-029/786	

Abstract (Basic): US 5477073 A

The appts. includes a **substrate** (21) with a thin film transistor (22) formed on it. The transistor is provided with a thin non-single crystalline **semiconductor** film with **channel** (22a), **source** and **drain regions** (22b). The **source** and **drain regions** are provided at opposite ends of the **channel region** and are highly doped with impurities of one conductivity type, e.g. **n-type**.

Two **low concentration** regions (22c) are also provided, one between the **channel** and **source region** and the other between the **channel** and **drain regions**. Each of the low concn. regions are lightly doped with impurities of the opposite conductivity type, e.g. **p-type**. The **channel region** is dopant free. A **gate insulation film** (23) is formed on the film **channel region** while a **gate electrode** (24) is formed on the **gate insulation film**. Respective **source** and **drain electrodes** (27) are connected to the **source** and **drain regions**.

USE/ADVANTAGE - Also for opto-electric converter and display driver. **Low concentration** region **impurities**, e.g. boron ions of **low concentration** 1 multiply 10¹³ atoms/cm², serve to reduce off current.

Dwg.1/7

09/12/2002 09/837,397

66/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010132300

WPI Acc No: 1995-033551/199505

XRAM Acc No: C99-131109

XRPX Acc No: N99-331717

MOS transistor production process - by forming shallow impurity diffusion having thin impurity density portion adjoining channel using **gate electrode** as mask

Patent Assignee: NEC CORP (NIDE)

Inventor: GOTO Y

Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6318699	A	19941115	JP 93128024	A	19930501	199505 B
US 5719430	A	19980217	US 94230778	A	19940421	199814
			US 96681516	A	19960723	
			US 96747745	A	19961112	
US 5933737	A	19990803	US 94230778	A	19940421	199938
			US 96681516	A	19960723	
			US 96747745	A	19961112	
			US 97895260	A	19970716	
KR 137625	B1	19980601	KR 949236	A	19940429	200015

Priority Applications (No Type Date): JP 93128024 A 19930501

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 6318699	A	10	H01L-029/784	
US 5933737	A	11	H01L-021/336	Cont of application US 94230778 Cont of application US 96681516 Div ex application US 96747745 Div ex patent US 5719430
US 5719430	A	10	H01L-029/76	Cont of application US 94230778 Cont of application US 96681516
KR 137625	B1		H01L-021/336	

Abstract (Basic): US 5933737 A

Abstract (Basic):

NOVELTY - A buried channel MOS transistor using ion implantation and diffusion to form **lower concentration of dopants** in the channel at the ends (24) of the gate (18) section than in the middle and thus reduce short channel effects.

DETAILED DESCRIPTION - A process for forming a buried-channel MOS transistor comprises introducing opposite dopant into a doped **semiconductor substrate** to form a buried channel layer (16) under a **gate dielectric** (14), forming a **gate electrode** (18) over the middle of the channel and introducing dopant into the end, unmasked, **channel regions** to form auxiliary diffused layers. Opposite dopant is introduced through these into the **substrate** in two steps to form **source** and **drain regions** (24,26), deeper than the channel layer and

incorporating a major part of them. An end portion of each auxiliary layer remains between an end of the middle region and the diffused layers of **source** and **drain** and the ends of the auxiliary region have **lower dopant concentrations** than the **middle region** of the buried **channel** layer.

USE - In forming buried-channel MOS transistors (claimed)

ADVANTAGE - Short-channel effects are reduced and the gate length can be 0.25 microns in a PMOS without punch-through; hot electron effects are also reduced and reliability increased.

DESCRIPTION OF DRAWING(S) - A cross-section of the MOS during processing is shown.

Gate dielectric (14)

Buried channel layer (16)

Gate electrode (18)

Diffused layers (24,26)

pp; 11 DwgNo 1D/6

Abstract (Equivalent): US 5719430 A

The process is applicable to an **n-type** silicon **substrate** (1). A **p-type** diffusion layer (4), gate oxide film (3) and a field oxide film (2) are formed on the **substrate**. An **n-type** polycrystal **gate electrode** (5) and a side oxide film (8) are installed on the above set-up. Ion implantation is carried out and a **p-type** diffusion layer (14) is formed. A **p-type** impurity diffusion layer (9) is formed to create **source** or **drain** domains using **gate electrode** as mask. The **substrate** is subjected to heat treatment and impurity layer is activated and a thin **p-type** diffusion layer (15) adjoining the **channel region** is formed. A **layer to layer insulation film** (10) in the metal wiring are formed.

ADVANTAGE - Increases effective channel length. Avoids short channel effect. Enables miniaturisation of device due to hot electron effect portion. Ensures high reliability.

Dwg.5c/6

66/3, AB/5 (Item 5 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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009872962
WPI Acc No: 1994-152875/199419
XRPX Acc No: N94-120076

MOS type **semiconductor device** - has bottom portion of
gate electrode side walls extending along surface of
semiconductor substrate
Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU); MATSUSHITA DENKI
SANGYO KK (MATU); MATSUSHITA ELECTRIC IND CO LTD (MATU)
Inventor: HIROKI A; KURIMOTO K; ODANAKA S

Number of Countries: 006 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 596468	A2	19940511	EP 93117804	A	19931103	199419	B
JP 6196495	A	19940715	JP 93275187	A	19931104	199433	
EP 596468	A3	19940629	EP 93117804	A	19931103	199527	
US 5512771	A	19960430	US 93147866	A	19931104	199623	
KR 9711744	B1	19970715	KR 9322967	A	19931101	199947	

Priority Applications (No Type Date): JP 92294820 A 19921104; JP 92294819 A
19921104

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 596468	A2	E 37	H01L-029/784	Designated States (Regional): DE FR GB
JP 6196495	A	20	H01L-021/336	
US 5512771	A	22	H01L-029/76	
EP 596468	A3		H01L-029/784	
KR 9711744	B1		H01L-021/336	

Abstract (Basic): EP 596468 A

The MOS type **semiconductor device** includes a **substrate** of one conductivity type doped with first conductivity type impurities. A MOS transistor is formed in it. The transistor has second conductivity type **drain** and **source regions**, and a pair of second type diffusion regions on either sides of a channel.

Side walls of a **gate electrode** have bottom portions which extend along the **substrates** surface from each side of the **electrode**. Each of the **source** and **drain regions** has a portion covered with a side wall, which is thinner than an uncovered portion. The covered portions reach a portion beneath each end of the **gate electrode**.

ADVANTAGE - Effective and accurate mfr. Reduced size. Avoids degrading characteristics. Exhibits high speed, high reliability and minimises short channel effects.

Dwg.1/17

Abstract (Equivalent): US 5512771 A
A complementary MOS type **semiconductor device**

comprising a **semiconductor substrate** including an **n-type** region doped with **n-type** impurities and a **p-type** region doped with **p-type** impurities and having a surface, an **n-channel MOS transistor** formed in said **p-type region**, and a **p-channel MOS transistor** formed in said **n-type region**, said **n-channel MOS transistor** including:

an **n-type source region** formed in said **p-type** region;

an **n-type drain region** formed in said **p-type** region and separated from said **n-type source region** by a first predetermined distance;

a first **channel region** formed in said **p-type** region and located between said **n-type source region** and said **n-type drain region**;

a pair of **n-type** impurity diffusion regions formed on both sides of said first **channel region** and having an **impurity concentration lower** than that of said **n-type source region**;

a first **gate insulating film** formed on said surface of said **semiconductor substrate**, said first **gate insulating film** directly covering said first **channel region** and said pair of **n-type** impurity diffusion regions, portions of said first **gate insulating film** above said pair of **n-type** impurity diffusion regions being thicker than a portion thereof above said first **channel region**; and

a first **gate electrode** formed on said first **gate insulating film**,

said **p-channel MOS transistor** including:

a **p-type source region** formed in said **n-type** region;

a **p-type drain region** formed in said **n-type** region and separated from said **p-type source region** by a second predetermined distance;

a second **channel region** formed in said **n-type** region and located between said **p-type source region** and said **p-type drain region**;

a second **gate insulating film** formed on said surface of said **semiconductor substrate** and having a uniform thickness; and

a second **gate electrode** formed on said second **gate insulating film**.

Dwg.11/17

09/12/2002 09/837,397

66/3,AB/6 (Item 6 from file: 350)
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008555429

WPI Acc No: 1991-059464/199109

XRAM Acc No: C91-025096

XRPX Acc No: N91-046074

MOSFET of LSS structure with sidewall spacers - which are from e.g.

N-type drains by P-type diffusion regions
from e.g. N-type drains by P-type diffusion
regions reducing hot carrier inject

Patent Assignee: NEC CORP (NIDE)

Inventor: NARITA K

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 414226	A	19910227	EP 90116095	A	19900822	199109	B
JP 3155662	A	19910703	JP 90216806	A	19900812	199133	
US 5170232	A	19921208	US 90571456	A	19900823	199252	
			US 91709818	A	19910604		
EP 414226	B1	19950419	EP 90116095	A	19900822	199520	
DE 69018734	E	19950524	DE 618734	A	19900822	199526	
			EP 90116095	A	19900822		

Priority Applications (No Type Date): JP 89218960 A 19890824; JP 90216806 A 19900812

*Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 414226 A

Designated States (Regional): DE FR GB
US 5170232 A 12 H01L-029/10 Cont of application US 90571456

EP 414226 B1 E 14 H01L-029/772

Designated States (Regional): DE FR GB
DE 69018734 E H01L-029/772 Based on patent EP 414226

Abstract (Basic): EP 414226 A

A MOS transistor has a **semiconductor substrate** (1) of a first conductivity type. On part of the **substrate** surface a **source** and **drain** (5.2 and 6.2) of a second conductivity type and on the inner sides of these another **source** and **drain pair** (5.1 and 6.1) of a lower concn. and depth than the first pair are formed. A **channel region** (a) is thus formed and a **gate electrode** (3) is provided above the channel (9) through an intermediate **insulating layer**. A pair of regions of the first conductivity type (7.1 and 8.1) are defined by layer (12) and formed on a partial surface of the second **source**, **drain pair**. Also provided are **sidewall spacers** (4) of insulating material, each at opposite sides of the **gate electrode** and above the regions of first conductivity type (7.1 and 8.1).

USE/ADVANTAGE - Useful in the mfr. of MOSFETS esp. LDD structures. The structure allows the **lower impurity** concn. layer to become buried so that peak electric field is relocated from the **substrate** surface. Therefore injection of hot carriers into

sidewall spacers is suppressed. (1pp Dwg.No.1G/2C)

Abstract (Equivalent): EP 414226 B

A MOS transistor comprising: a first source layer and a first **drain** layer formed with a space therebetween on the surface in a one-conductivity-type part of a **semiconductor substrate**, said first **source/drain** layers having a conductivity type opposite to said one-conductivity-type; a pair of second **source/drain** layers formed on the surface in said one-conductivity-type part of said **semiconductor substrate** to be opposed to each other with a region remaining at respective inner sides of said first **source/drain** layers, said second **source/drain** layers being smaller in depth and **lower in impurity concentration** than said first **source/drain** layers, a **gate electrode** formed above said remaining region in said one-conductivity-type part of said **semiconductor substrate** through the intermediate of a **gate-insulating layer**; and a pair of sidewall **spacers** of insulating material each formed above said pair of one-conductivity-type regions, respectively, and flanked with the opposite sides of said **gate electrode**, respectively; characterised in that a pair of regions of said one conductivity-type is formed to be on a partial surface of said second **source/drain** layers, respectively, and is separated from said remaining region.

Dwg.0/2

Abstract (Equivalent): US 5170232 A

The MOS transistor comprises (a) 1st **source** and 1st **drain** layer formed into the surface of a 1st conductivity type part of a **substrate** in opposing, spaced relation, the layers having opposite conductivity, (b) 2nd **source** and **drain** layers of opposite conductivity in spaced apart relation formed into the surface of the **substrate**, with their outer side surfaces being adjacent the inner side surface of the 1st layers, the 2nd layers being smaller in depth and **lower in impurity concn.**, (c) a pair of 1st type regions between the 1st and 2nd **source** and **drain** layers, (d) a **gate electrode** on a **gate insulating layer** above a remaining portion of the **substrate** between the inner side surfaces of the 1st **source drain** layers, and (e) a pair of **insulating sidewall spacers** in self-aligned, overlying relation above the 1st type regions and adjacent a respective opposing side of the **gate electrode**.

USE/ADVANTAGE - Used for an LDD type MOSFET. The undesirable effect of hot carriers are minimised.

Dwg.1g/2

09/12/2002 09/837,397

66/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007431451
WPI Acc No: 1988-065386/198810
XRAM Acc No: C88-029251
XRPX Acc No: N88-049528

P-channel MOS transistor with double diffused **drain** and
source - has reduced diffusion resistance and gate to diffusion
overlap capacitance

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: HIEDA K; NITAYAMA A; SUNOUCHI K; TAKENOUCHI N; TSUDA K; TAKATO H

Number of Countries: 004 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3728849	A	19880303	DE 3728849	A	19870828	198810	B
JP 63058872	A	19880314	JP 86201706	A	19860829	198816	
JP 63283152	A	19881121				198902	
JP 63283155	A	19881121				198902	
US 5164801	A	19921117	US 8790021	A	19870827	199249	
			US 89339930	A	19890419		
			US 89445152	A	19891205		
			US 91668378	A	19910311		
			US 91790066	A	19911112		
DE 3728849	C2	19950713	DE 3728849	A	19870828	199532	

Priority Applications (No Type Date): JP 87118317 A 19870515; JP 86201706 A
19860829; JP 87118316 A 19870515

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3728849	A	25			Cont of application US 8790021
US 5164801	A	25	H01L-027/14		Cont of application US 89339930
					Cont of application US 89445152
					Cont of application US 91668378
DE 3728849	C2	25	H01L-029/772		

Abstract (Basic): DE 3728849 A

The transistor, with **gate-electrode** (31), pref. smaller than 1 micron, on a **gate-insulator layer** (32), has **source/drain regions** consisting of 2 parts : a **low doping level diffusion region** (33,34) at the top, and completely surrounding this, a higher doping level region (35,36). The transistor is then completed with **source/drain metallisation**. (40,41).

The junctions formed by both regions with the **substrate**, sideways in the gate-area, are pref. coincident. The depth of the heavily doped region is pref. more than that of the slightly dopes region. The regions are pref. made by ion-implantation, pref. of B, in an **n-type substrate** followed by diffusion or anneal.

In the mfr. the surface area of the **low doping level**

implant is pref. defined on the channel side by the **gate-electrode** (31). That of the highly doped implant by the **gate-electrode spacer-oxide** (38). The P-MOS transistors can also be mfd. in CMOS and/or BiCMOS processes. In that case the n-channel transistors are pref. built traditionally with LD-drain and **source regions** using As for the highly doped and P as impurity for the lightly doped region.

USE/ADVANTAGE - The process results in reduced diffusion series-resistance, e.g. by about 200 ohms. The overlap capacitance of gate to diffusion is also reduced e.g. by about 50%. This results in transistors suitable for higher operating frequency.

/14

Abstract (Equivalent): DE 3728849 C

A metal isolated **semiconductor**, MIS, transistor device has an 'n' type region (30) onto which a gate isolation layer (32) is formed and supports a **gate electrode** (31). The **source** and **drain** (22,34,35,36) regions are formed with the former having a **higher foreign atom concentration**. **Source** and **drain electrodes** (40,41) are formed on top of these surfaces. The one region (35,36) has edge regions extending beyond those of the other (33,34) and are of a greater depth. A 'P' **channel implanted region** is formed on the surface of the 'n' type **substrate** (30).

USE/ADVANTAGE - Form and mfr. reduces stray resistance.

Dwg.3/4

Abstract (Equivalent): US 5164801 A

A P channel MIS type **semiconductor** comprising an N type **substrate** on which is applied a **gate insulating layer** with a **channel region** below the insulation and a **gate electrode** above. **Source** and **drain regions** are formed by doping the **substrate** on opposite sides of the channel. The channel side edge of the first region is on or outside the edge of the second region. The second region having a **higher concentration of impurity** than the first region in an area along the surface of the **source** and **drain regions**. ADVANTAGE - The device has decreased parasitic resistance. (Dwg.5B/14

09/12/2002 09/837,397

66/3,AB/8 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO
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06630341
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 2000-216155 [JP 2000216155 A]
PUBLISHED: August 04, 2000 (20000804)
INVENTOR(s): KADOKURA SHOZO
APPLICANT(s): SONY CORP
APPL. NO.: 11-012382 [JP 9912382]
FILED: January 20, 1999 (19990120)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent phosphorus from diffusing from a PSG film so as to enable a P channel-type transistor to operate at a high speed, by a method wherein a phosphorus-free glass **substrate** is formed as an interlayer **insulating film** on all the surfaces of a **gate electrode** on a **gate insulating film** provided to a **substrate** and a **source region** and a **drain region** on the surface of the **substrate**.

SOLUTION: A **gate electrode** 3 is formed on an **N-type substrate** 1 through the intermediary of a gate oxide film 2, and a **gate capping insulating film** 5 is formed on the side of the **gate electrode** 3. A **P-type LDD region** 6 which contains **P-type impurities** of comparatively low concentration, and **P-type source/drain regions** 7 which contain **P-type impurities** of comparatively high concentration, are formed on the surface of the **N-type substrate** 1 so as to form a **channel region** under the **gate electrode** 3. Then, an interlayer **insulating film** 8 of non-doped silicate glass is formed on all the surface so as to cover a side wall 4 and the **gate capping film** 5.

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66/3,AB/9 (Item 9 from file: 347)
DIALOG(R) File 347:JAPIO
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06610168

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-195973 [JP 2000195973 A]
PUBLISHED: July 14, 2000 (20000714)
INVENTOR(s): NOGUCHI OSAMU
APPLICANT(s): SONY CORP
APPL. NO.: 10-371633 [JP 98371633]
FILED: December 25, 1998 (19981225)

ABSTRACT

PROBLEM TO BE SOLVED: To suppress current path generated by deposited phosphorous in a **semiconductor device**, by forming on a first polysilicon layer of its floating **gate electrode** an impurity-diffusion adjusting film, and by forming on a second **insulation film** of the impurity-diffusion adjusting film a second polysilicon layer which contains a **higher concentration impurity** than the first polysilicon layer.

SOLUTION: An N-channel MOS transistor comprises p-channel regions 103 formed on an n-type semiconductor substrate 101, a first **insulation film** (gate oxide film) 105, formed on an N-channel region present in the region partitioned by element separating films 104, a floating **gate electrode** 106 formed via the film 105, a second **insulation film** 109 formed on the **electrode** 106 and having a three-layer structure of silicon oxide/silicon nitride/silicon oxide layers, and a control gate having a laminated structure of a phosphorous-impurity containing second polysilicon layer 110 and a tungsten silicide layer 111. Furthermore, in the N-channel MOS transistor, a protective films 114 are provided on both the sidewall portions of its **gate electrode**, and in the lower peripheral region of each protection film 114, an n--impurity diffusing region 112 having an n-type relatively low-concentration diffused **impurity** is formed, and further in the peripheral region of each region 112, a source/drain region 113 having an n-type high-concentration diffused **impurity** is formed.

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66/3,AB/10 (Item 10 from file: 347)
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04037927

THIN FILM TRANSISTOR AND MANUFACTURE THEREOF

PUB. NO.: 05-029627 [JP 5029627 A]
PUBLISHED: February 05, 1993 (19930205)
INVENTOR(s): TAKEDA KOJI
TOSAKA HISAO
APPLICANT(s): CASIO COMPUT CO LTD [350750] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 03-201195 [JP 91201195]
FILED: July 17, 1991 (19910717)
JOURNAL: Section: E, Section No. 1381, Vol. 17, No. 313, Pg. 35, June
15, 1993 (19930615)

ABSTRACT

PURPOSE: To decrease a cutoff current sufficiently without the large effect on an ON current.

CONSTITUTION: A ground **insulating thin film** 2 is provided on the upper surface of a **substrate** 1. A cutoff-current suppressing layer 3 is provided on the upper surface of the ground **insulating thin film** 2. A **semiconductor thin film** 4 comprising polysilicon is provided at the specified part of the cutoff-current suppressing layer 3. A **gate insulating film** 5 is provided on the **semiconductor thin film** 4 and the cutoff-current suppressing layer 3. A **gate electrode** 7 is provided on the upper surface of the **gate insulating thin film** 5 of a part corresponding to a **channel region** 6 of the **semiconductor thin film** 4. **Source and drain regions** 8 wherein **high-concentration impurities** are contained are provided at the **semiconductor thin film** 4 at both sides of the **gate electrode** 7. The cutoff-current suppressing layer 3 comprises amorphous silicon wherein impurities of the conductivity type that is opposite to the **source and drain regions** (p-type impurities when the **source and drain regions** 8 are n-type, and n-type impurities when the regions 8 are p-type) are contained.

66/3,AB/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
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04004171
THIN FILM TRANSISTOR

PUB. NO.: 04-369271 [JP 4369271 A]
PUBLISHED: December 22, 1992 (19921222)
INVENTOR(s): TAKEDA KOJI
WAKAI HARUO
APPLICANT(s): CASIO COMPUT CO LTD [350750] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 03-170438 [JP 91170438]
FILED: June 17, 1991 (19910617)
JOURNAL: Section: E, Section No. 1365, Vol. 17, No. 245, Pg. 156, May
17, 1993 (19930517)

ABSTRACT

PURPOSE: To sufficiently reduce a cutoff current without affecting large influence to an ON current.

CONSTITUTION: A base insulating thin film 2 is provided on an upper surface of a substrate 1. A cutoff current suppressing layer 3 is provided on the upper surface of the film 2. A semiconductor thin film 4 made of polysilicon, etc., is provided at a predetermined position on the upper surface of the layer 3. A gate insulating film 5 is provided on the upper surfaces of the film 4 and the layer 3. A gate electrode 7 is provided on the upper surface of the film 5 of a part corresponding to a channel region 6 of the film 4. Source/drain regions 8 containing high concentration impurity are provided on the film 4 at both sides of the electrode 7. The layer 3 is formed of a semiconductor thin film made of polysilicon, etc., containing opposite conductivity type impurity (p-type impurity in the case that the regions 8 are n-type or n-type impurity in the case where the regions 8 are p-type) to those of the regions 8.

09/12/2002 09/837,397

66/3,AB/12 (Item 12 from file: 347)
DIALOG(R) File 347:JAPIO
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03987266

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 04-352366 [JP 4352366 A]
PUBLISHED: December 07, 1992 (19921207)
INVENTOR(s): MITSUI KATSUKICHI
KUSUNOKI SHIGERU
INUISHI MASAHIKE
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-155903 [JP 91155903]
FILED: May 29, 1991 (19910529)
JOURNAL: Section: E, Section No. 1357, Vol. 17, No. 214, Pg. 75, April 27, 1993 (19930427)

ABSTRACT

PURPOSE: To reduce the frequency of the scattering of impurities of conductive carriers in a **channel region** and to restrain a drop in a mobility due to the scattering of the impurities of the conductive carriers by a method wherein one part of a single-crystal first-conductivity-type **semiconductor substrate** at a low **impurity concentration** is used as the surface of the **channel region** coming into contact with a **gate insulating film**.

CONSTITUTION: N-type impurities are implanted deep into a P-type **semiconductor substrate** 1 by a high-energy ion implantation method; an **N-type well** 2 is formed. Part of the **P-type semiconductor substrate** 1 is left on the **N-type well** 2. The one part, of the **P-type semiconductor substrate** 1, which has been left on the **N-type well** 2 is used as a **P-type channel region**; a **gate insulating film** 4 and a **gate electrode** 5 are formed on its surface; and a **source-drain region** is formed. Since the **impurity concentration** of the **P-type substrate** 1 is low in this manner, the **impurity concentration** is low even in the **P-type channel region** using it. Consequently, a drop in a mobility due to the scattering of impurities of **conductive carriers** and the deterioration of the performance of a device itself due to it are not caused.

66/3,AB/13 (Item 13 from file: 347)
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03593463

SEMICONDUCTOR DEVICE

PUB. NO.: 03-256363 [JP 3256363 A]
PUBLISHED: November 15, 1991 (19911115)
INVENTOR(s): HAYAMA MASAHIRO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 02-055453 [JP 9055453]
FILED: March 06, 1990 (19900306)
JOURNAL: Section: E, Section No. 1166, Vol. 16, No. 59, Pg. 6,
February 14, 1992 (19920214)

ABSTRACT

PURPOSE: To improve the breakdown strength between a **source** and a **drain** and to arrange that other electrical characteristics are hardly affected by a method wherein parts of a **gate electrode** which traverses upper parts of diffusion layers, for inner-element leakage prevention use, situated at both ends in the width direction of a **channel region** are made thicker than a part situated on the **channel region**.

CONSTITUTION: A **source region** S and a **drain region** D are formed, by diffusing, e.g. **N-type** impurities, so as to sandwich a **channel region**. Diffusion layers 2, 2, for leakage-current prevention use, of **high-concentration impurities** whose conductivity type is the same as that of a **substrate** 1 are formed at both ends in the width direction (direction perpendicular to the direction between the **source** and the **drain**) of the **channel region**; a **gate electrode** 4 is formed on the **channel region** via a **gate insulating film** 3. The **gate electrode** 4 is extended up to upper parts of the **P-type** diffusion layers 2 for leakage-current prevention use. The size in the gate length direction of extended parts is expanded to both sides before the expanded parts enter the upper parts of the **P-type** diffusion layers 2; the **gate electrode** traverses the upper parts of the **P-type** diffusion layers 2 in the expanded size.

66/3,AB/14 (Item 14 from file: 347)
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03350067

MANUFACTURE OF INSULATING-GATE FIELD-EFFECT TRANSISTOR

PUB. NO.: 03-012967 [JP 3012967 A]
PUBLISHED: January 21, 1991 (19910121)
INVENTOR(s): INOUE SHIGETO
APPLICANT(s): SEIKO INSTR INC [000232] (A Japanese Company or Corporation),
JP (Japan)
APPL. NO.: 01-149074 [JP 89149074]
FILED: June 12, 1989 (19890612)
JOURNAL: Section: E, Section No. 1050, Vol. 15, No. 125, Pg. 145,
March 27, 1991 (19910327)

ABSTRACT

PURPOSE: To prevent an electron trap and a hole trap from being produced in a **gate insulating film** by selecting a crystal face orientation, along which the largest number of impurities diffuse, as the direction from a **source** to a **drain** when the **source** and **drain regions** are formed.

CONSTITUTION: An N^(sup +) **source region** 3 and an N^(sup +) **drain region** 1 are formed on both sides of the P type channel region of P type Si substrate 5 and a **gate insulating film** 6 and a **gate electrode** 2 are formed on said P type channel region. Impurities thermally diffuse from the N^(sup +) **source region** 3 and the N^(sup +) **drain region** 1 by high-temperature processing to form N^(sup -) low-concentration **impurity regions** 4. In this high-temperature processing, face {100} is selected as the direction from the **source** to the **drain**, therefore, the desired N^(sup -) low- concentration **impurity regions** 4 are obtained in a short time. Thereby production of an electron trap and a hole trap in the **gate insulating film** can be prevented.

66/3,AB/15 (Item 15 from file: 347)
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03135473

MOS TYPE SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 02-110973 [JP 2110973 A]
PUBLISHED: April 24, 1990 (19900424)
INVENTOR(s): FUKUDA ETSUO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-263147 [JP 88263147]
FILED: October 19, 1988 (19881019)
JOURNAL: Section: E, Section No. 952, Vol. 14, No. 328, Pg. 55, July
13, 1990 (19900713)

ABSTRACT

PURPOSE: To obtain a MOS **semiconductor device** which is micronized in structure, high in breakdown strength against punch-through, and reduced in a short channel effect by a method wherein a semicylindrical recessed part is formed on the surface of a **semiconductor substrate**, and a MOS transistor, whose structure is such that a **gate electrode** 4 is provided to the recessed part through the intermediary of **gate insulating film**, is provided.

CONSTITUTION: A MOS type **semiconductor device** of this design is possessed of a MOS transistor, which is composed of a semicylindrical recessed part 2 formed on the surface of a **semiconductor substrate** 1, a **gate electrode** 4 formed to be buried in the recessed part 2 through the intermediary of a **gate insulating film** 3, and **source** and **drain** layers 5(sub 1), 6(sub 1), 5(sub 2), 6(sub 2) formed being self-aligned with the **gate electrode** 4. For instance, the **channel region** of a **P-type Si substrate** is processed to be provided with a recessed part 2, the **gate electrode** 4 is formed to be buried in the recessed part 2 through the intermediary of the **gate insulating film** 3, and the **source** and the **drain** layer are formed at the ends of the semicylindrical recessed part 2 being self-aligned with the **gate electrode** 4. And, the **source** and the **drain** layer are composed of **low impurity concentration** n^(sup -)-type layers 5(sub 1) and 5(sub 2) and **high impurity concentration** n^(sup +)-layers 6(sub 1) and 6(sub 2) positioned above the layers 5(sub 1) and 5(sub 2) to constitute an LDD structure.

66/3,AB/16 (Item 16 from file: 347)
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02914377

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE

PUB. NO.: 01-211977 [JP 1211977 A]
PUBLISHED: August 25, 1989 (19890825)
INVENTOR(s): SHIBATA TAKASHI
UCHIDA KEN
TAKEDA TOSHIKUMI
MATSUMOTO YOICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-035206 [JP 8835206]
FILED: February 19, 1988 (19880219)
JOURNAL: Section: E, Section No. 848, Vol. 13, No. 518, Pg. 166,
November 20, 1989 (19891120)

ABSTRACT

PURPOSE: To prevent short channel effect, by forming the low concentration region on the channel region side of a drain, by using impurity whose diffusion coefficient is small as compared with phosphorus.

CONSTITUTION: A P-type semiconductor region 51 is formed from the main surface of a semiconductor substrate 1 toward the inside, and gate electrodes 10 are formed on the main surface, putting a gate insulating film 9 therebetween. Arsenide ion is introduced by using the electrodes 10 as a mask, and a first semiconductor region 11 of N-type is formed in the P-type semiconductor region 51. Side walls 13 are arranged on both side walls of the gate electrode 10. Arsenide ion is introduced by arranging side walls 13 on both side walls of the gate electrodes 10 and using the gate electrodes 10 and the side wall 13 as masks. Electric connection with the first semiconductor region 11 is completed, and a second semiconductor region 12 of high impurity concentration is formed. The low concentration region 11 of a source/drain region is formed, in the above manner, by using arsenide whose diffusion coefficient is small, thereby reducing the oozing into the channel region, and preventing short channel effect.

09/12/2002 09/837,397

66/3,AB/17 (Item 17 from file: 347)
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02661373

SEMICONDUCTOR DEVICE

PUB. NO.: 63-278273 [JP 63278273 A]
PUBLISHED: November 15, 1988 (19881115)
INVENTOR(s): HAZAMA HIROAKI
APPLICANT(s): AGENCY OF IND SCIENCE & TECHNOL [000114] (A Japanese
Government or Municipal Agency), JP (Japan)
APPL. NO.: 62-098730 [JP 8798730]
FILED: April 23, 1987 (19870423)
JOURNAL: Section: E, Section No. 726, Vol. 13, No. 106, Pg. 115, March
14, 1989 (19890314)

ABSTRACT

PURPOSE: To suppress a **substrate** potential without expanding a device area and to efficiently collect an excess carrier generated inside a **semiconductor** film by forming a **semiconductor** region which functions as a **substrate electrode** which comes into contact with both a **source region** and a **channel region**.

CONSTITUTION: A silicon oxide film is deposited on a silicon **substrate** 11; a polycrystalline silicon film doped with a **p-type** impurity is deposited on it. In succession, this film is transformed to be single-crystalline; a **P-type** single-crystal silicon film 13 is formed. Then, a device formation region is patterned like an island; a **gate insulating film** 14 is formed by a thermal oxidation method; a **gate electrode** 15 is formed and patterned. Then, ions of boron are implanted into only the lower part of a **source region**; a **substrate electrode** 16 as a **p⁺ impurity** layer of high concentration is formed. Then, ions are implanted in order to form a **source region** 17 and a **drain region** 18. Then, a CVD oxide film 21 is deposited on the whole surface; a contact hole which reaches the **source region**, the **drain region** and the **gate region** is formed; a wiring operation is executed by using metal wiring parts 22.

66/3,AB/18 (Item 18 from file: 347)
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02612958

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 63-229858 [JP 63229858 A]
PUBLISHED: September 26, 1988 (19880926)
INVENTOR(s): ARAKI MINORU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 62-066566 [JP 8766566]
FILED: March 19, 1987 (19870319)
JOURNAL: Section: E, Section No. 707, Vol. 13, No. 31, Pg. 2, January
24, 1989 (19890124)

ABSTRACT

PURPOSE: To contrive the speedup of operation of a **semiconductor device**, an increase in the density of the device and the improvement of reliability of the device by a method wherein an impurity layer having a conductivity type inverse to that of a **semiconductor substrate** is formed in the **substrate** surface to bore a groove and impurity diffused layers having a conductivity type inverse to that of the **substrate** are provided separately from a **gate electrode** for filling the groove.

CONSTITUTION: An **n-type** epitaxial layer 103, which is an impurity layer having a conductivity type inverse to that of a **p-type semiconductor substrate** 101, is formed in the surface of the **substrate** 101, a groove 113 to reach the **substrate** 101 is bored and is used as a **channel region** and at the same time, the layer 103 is halved by the groove 113 to form **drain** and **source regions**. A **gate electrode** 108 is buried in the groove 113 through a **high-concentration p⁺ impurity region** 105 on the bottom part of this groove 113 and a **gate insulating film** 106 to reach the surface of the layer 103. Moreover, **high-concentration n⁺** diffused layers 109 and 110 having a conductivity type inverse to that of the **substrate** 101 are formed in the layer 103 separately from the edge end parts of the **electrode** 108. By this constitution, the injection of electrons into the film 106 is inhibited, the electric capacities of the layers 109 and 110 are decreased and the operation of a **semiconductor device** can be speeded up. Moreover, the channel length is decided by tie width and depth of the groove, an increase in the density of the device can be contrived and the reliability of the device can be improved.

66/3,AB/19 (Item 19 from file: 347)
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02161979

MOS SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 62-078879 [JP 62078879 A]
PUBLISHED: April 11, 1987 (19870411)
INVENTOR(s): HARA TOSHIO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-218367 [JP 85218367]
FILED: September 30, 1985 (19850930)
JOURNAL: Section: E, Section No. 539, Vol. 11, No. 280, Pg. 47,
September 10, 1987 (19870910)

ABSTRACT

PURPOSE: To obtain a highly integrated circuit device, by utilizing, as a channel region of an MOS transistor, the bottom face of a source/drain electrode consisting of two layers having different impurity concentrations and the bottom face of a gate electrode located in a position deeper than the depth of the junction between the source and the drain.

CONSTITUTION: A source/drain semiconductor layer having a two-layer structure consisting of an N^{sup +} type semiconductor layer 3 with a high concentration of an N-type impurity and an N^{sup -} type semiconductor layer 2 with a low concentration of an impurity is provided on one principal surface of a P-type semiconductor substrate 1. The source/drain semiconductor layer is connected to a metallic wiring layer 8 through an aperture in an insulation film 7 covering the surface of the substrate. A gate electrode 5 is buried in the layers and a gate insulation film 6 is formed on the surface of the gate electrode for providing an N-channel MOS transistor. The effective length of the channel of this transistor is the length as measured along the interface between the N^{sup -} type semiconductor layer 2 and the semiconductor substrate 1 and along the surface of the semiconductor substrate 1 located on the bottom of the gate electrode, and that length is larger than the width of the gate electrode 5.

66/3,AB/20 (Item 20 from file: 347)
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01930777

PRODUCTION OF SEMICONDUCTOR DEVICE

PUB. NO.: 61-144877 [JP 61144877 A]
PUBLISHED: July 02, 1986 (19860702)
INVENTOR(s): MATSUMURA HOMARE
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 59-267935 [JP 84267935]
FILED: December 19, 1984 (19841219)
JOURNAL: Section: E, Section No. 455, Vol. 10, No. 340, Pg. 158,
November 18, 1986 (19861118)

ABSTRACT

PURPOSE: To obtain a **semiconductor device** with low-melting point metallic gate which is capable of high-speed switching operation and suited for miniaturization, by a method wherein a gate is formed on an opening after the mask layer at the time of ion injection has been removed so as to form **source** and **drain diffusion layers** and a **gate electrode** self-matchingly.

CONSTITUTION: An **insulation film** 2 of SiO₂ is formed on a **p type Si substrate**, and an opening is partially opened on the film to form an element region. The region is heat-oxidized to form an **insulation film** 3 to evaporate Al on the film. Then, the Al is removed to form a mask layer 4 of Al with the photoetching method on the part which is to be a **channel region**. As is ion-injected to form a **high-concentration n type impurity** layer 5. An inter-layer insulation film 6 is formed, and a mask layer 4 is exposed with flattening etching method. Then, the layer 4 and lower insulation layer of SiO₂ are removed to form a **gate insulation film** 7 of SiO₂ on this part. An opening is opened on the film 6 on the layer 5 to form a contact hole 10, and Al is evaporated over the surface, and a **source electrode**, **drain electrode** 8, and **gate electrode** 9 are formed to obtain a MOST.

66/3, AB/21 (Item 21 from file: 347)
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01906372

MANUFACTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 61-120472 [JP 61120472 A]
PUBLISHED: June 07, 1986 (19860607)
INVENTOR(s): KURODA KENICHI
KOMORI KAZUHIRO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 59-240618 [JP 84240618]
FILED: November 16, 1984 (19841116)
JOURNAL: Section: E, Section No. 446, Vol. 10, No. 306, Pg. 98,
October 17, 1986 (19861017)

ABSTRACT

PURPOSE: To obtain an FET, which is operated at a high speed and is not subject to insulation breakdown, when the FET, in which floating and control **electrodes** are laminated, by using **low impurity concentration** Si for the floating **electrode** so that an SiO₂ film that is to become an interlayer **insulating film** is yielded by heat treatment, and using a laminated body of **high concentration** Si and a **high-melting-point metal** for the control **electrode**.

CONSTITUTION: An FET, in which a floating **gate electrode** 5A and a control **gate electrode** 7A are laminated through an interlayer **insulating film** 6A, is formed, and one constituent element of an EPROM is provided. At this time, at first, a field **insulating film** 2 is formed on a **p type channel stopper region** 3 on a p⁻ type Si **substrate** 1. Then n⁺ type **source and drain regions** 9A are formed on the surface layer part of the **substrate** 1. The floating **gate electrode** 5A comprising **low impurity concentration** Si is formed between the regions 9A through a **gate insulating film** 4A. Thereafter, heat treatment is performed, and the surface layer is converted into an SiO₂ layer 6A, which is to become an interlayer **insulating film**. The control **gate electrode** 7A, which comprises a laminated body of **high impurity concentration** Si, Mo and the like, is laminated on the film 6A.

66/3,AB/22 (Item 22 from file: 347)
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01904978

MOS SEMICONDUCTOR DEVICE

PUB. NO.: 61-119078 [JP 61119078 A]
PUBLISHED: June 06, 1986 (19860606)
INVENTOR(s): HARADA HIROSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 59-240222 [JP 84240222]
FILED: November 14, 1984 (19841114)
JOURNAL: Section: E, Section No. 446, Vol. 10, No. 306, Pg. 73,
October 17, 1986 (19861017)

ABSTRACT

PURPOSE: To prevent the generation of short channel effect and to prevent the decline of **conductance** by forming a **gate electrode** in a manner it covers the overall surface of a **low-concentration impurity layer** and a **channel region**.

CONSTITUTION: On a surface of a **P type silicon substrate** 21, **N^{sup +}** layers 22 and 23 which become **source** and **drain** respectively are formed and the **N^{sup -}** layers 24 and 25 are formed respectively on the channel side in the vicinity of the **N^{sup +}** layers 22 and 23. These **N^{sup -}** layers 24 and 25 are **low-concentration impurity** layers for alleviating an electric field in an LDD structure and both are formed more thinly than the **N^{sup +}** layers 22 and 23. On a surface of the silicon **substrate** 21, a **gate electrode** 26 is arranged through a **gate insulating film** 26 and the **gate electrode** 26 extends its ends to the internal ends of the **N^{sup +}** layers 22 and 23 to become **source** and **drain** and it covers the overall surface of a **channel region** and the **N^{sup -}** layers 24 and 25.

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Set	Items	Description
S1	5192	AU=(KIKUCHI, S? OR KIKUCHI S?)
S2	43	AU=(NISHIBE, E? OR NISHIBE E?)
S3	63213	AU=(SUZUKI, T? OR SUZUKI T?)
S4	59	S1 AND S3
S5	23	S4 AND S2
S6	16	S5 AND SEMICONDUCT?????
S7	1	S6 AND (ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????)
S8	15	S6 NOT S7
S9	7	S5 NOT S6
S10	0	S9 AND SUBSTRATE? ?
S11	0	S9 AND ((INSULAT?????? OR DIELECTRIC???) (3N) (LAYER??? OR F- ILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S12	4	RD S9 (unique items)
S13	36	S4 NOT S5
S14	0	S13 AND ((INSULAT?????? OR DIELECTRIC???) (3N) (LAYER??? OR - FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S15	1	S13 AND SEMICONDUCT?????
S16	107	S1 AND SEMICONDUCT?????
S17	12	S16 AND (ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????)
S18	2	S17 AND SUBSTRATE? ?
S19	10	S17 NOT S18
S20	1	S19 AND ((HIGH OR LOW OR LOWER) (3N) (DOPE???? OR DOPA???? OR DOPE???? OR DOPA?????? OR DOPING OR IMPURIT??????))
S21	9	S19 NOT S20
S22	5	RD (unique items)

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7/3,AB/1 (Item 1 from file: 94)
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04049339 JICST ACCESSION NUMBER: 99A0391971 FILE SEGMENT: JICST-E
Microelectronic Test Structures. High-Voltage MOS Device Modeling with
BSIM3v3 SPICE Model.

MYONO T (1); NISHIBE E (1); KIKUCHI S (1); IWATSU K (1);
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IEICE Trans Electron(Inst Electron Inf Commun Eng), 1999, VOL.E82-C,NO.4,
PAGE.630-637, FIG.10, TBL.1, REF.13

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ABSTRACT: This paper presents a new technique for modeling High-Voltage
lightly-doped-drain MOS (HV MOS) devices accurately with the BSIM3v3
SPICE model. Standard SPICE models do not model the voltage dependency
of Rs and Rd in HV MOS devices; this causes large discrepancies between
the simulated and measured I-V characteristics of HV MOS devices. We
propose to assign physical meanings and values different from the
original BSIM3v3 model to three of its parameters to represent the
voltage dependency of Rs and Rd. With this method, we have succeeded in
highly accurate parameter extraction, and the simulated I-V
characteristics of HV MOS devices using the extracted parameters match
the measured results well. The relationship between the proposed
modeling technique and the physical mechanism of HV MOS devices is also
discussed based on measurement and device simulation results. Since our
method does not change any model equations of BSIM3v3, it can be
applied to any SPICE simulator on which the BSIM3v3 model runs, so we
can use SPICE simulation for accurate circuit design of complex
circuits using HV MOS devices. (author abst.)

09/12/2002

8/3,AB/1 (Item 1 from file: 2)

DIALOG(R) File 2:INSPEC

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6564898 INSPEC Abstract Number: B2000-05-2560R-093, C2000-05-7410D-124
Title: Modeling and parameter extraction technique for uni-directional HV
MOS devices

Author(s): Myono, T.; Nishibe, E.; Kikuchi, S.; Iwatsu, K.;
Suzuki, T.; Sasaki, Y.; Itoh, K.; Kobayashi, H.

Author Affiliation: MOS-LSI Div., Sanyo Electr. Co. Ltd., Gunma, Japan
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Conference Date: 19-20 April 1999 Conference Location: Karuizawa,
Japan

Language: English

Abstract: This paper presents a new technique for accurately modeling
uni-directional high-voltage lightly-doped-drain MOS (HV MOS) devices by
extending the bi-directional HV MOS model and adopting a new parameter
extraction method. We have already reported on a SPICE model for
bi-directional HV MOS devices based on BSIM3v3. However, if we apply this
bi-directional HV MOS model and its parameter extraction technique directly
to uni-directional HV MOS devices, there are large discrepancies between
the measured and simulated I-V characteristics of the uni-directional
devices. This paper extends the bi-directional HV MOS model, and adopts a
new parameter extraction technique. Using parameters extracted with the new
method, the simulated I-V characteristics of the unidirectional n-channel
HV MIOS device match the measured results well. Since our method does not
change any model equations of BSIM3v3, it can be applied to any SPICE
simulator on which the BSIM3v3 model runs.

Subfile: B C

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8/3,AB/2 (Item 2 from file: 2)

DIALOG(R) File 2:INSPEC

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6460013 INSPEC Abstract Number: B2000-02-2560P-005, C2000-02-7410D-103

Title: Modeling and parameter extraction technique for high-voltage MOS device

Author(s): Myono, T.; Nishibe, E.; Kikuchi, S.; Iwatsu, K.;
Suzuki, T.; Sasaki, Y.; Itoh, K.; Kobayashi, H.

Author Affiliation: Sanyo Electr. Co. Ltd., Japan

Conference Title: ISCAS'99. Proceedings of the 1999 IEEE International Symposium on Circuits and Systems VLSI (Cat. No.99CH36349) Part vol.6 p.230-3 vol.6

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 1999 Country of Publication: USA 6 vol.
(liv+565+717+568+604+647+527) pp.

ISBN: 0 7803 5471 0 Material Identity Number: XX-1999-01885

U.S. Copyright Clearance Center Code: 0 7803 5471 0/99/\$10.00

Conference Title: ISCAS'99. Proceedings of the 1999 IEEE International Symposium on Circuits and Systems. VLSI

Conference Date: 30 May-2 June 1999 Conference Location: Orlando, FL, USA

Language: English

Abstract: This paper presents a novel technique for modeling HV MOS devices accurately with the BSIM3v3 SPICE model. We assign different meanings from the original BSIM3v3 to three parameters. The simulated I-V characteristics using the extracted parameters match the measured results well, and the physical mechanism of HV MOS devices is clarified based on device simulations. Since our method does not change any model equations of BSIM3v3, it can be applied to any SPICE simulator on which the BSIM3v3 model runs.

Subfile: B C

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8/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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6321476 INSPEC Abstract Number: B1999-09-2560R-060, C1999-09-7410D-098
Title: Modelling technique for uni-directional HV MOS devices based on
BSIM3v3

Author(s): Myono, T.; Nishibe, E.; Kikuchi, S.; Iwatsu, K.;
Suzuki, T.; Sasaki, Y.; Itoh, K.; Kobayashi, H.

Author Affiliation: MOS-LSI Div., Sanyo Electr. Co. Ltd., Gunma, Japan
Journal: Electronics Letters vol.35, no.14 p.1200-1

Publisher: IEE,

Publication Date: 8 July 1999 Country of Publication: UK

CODEN: ELLEAK ISSN: 0013-5194

SICI: 0013-5194(19990708)35:14L.1200:MTDD;1-J

Material Identity Number: E089-1999-014

U.S. Copyright Clearance Center Code: 0013-5194/99/\$10.00

Language: English

Abstract: A SPICE model for bi-directional HV MOS devices based on
BSIM3v3 is extended by adopting a new parameter extraction method for
modelling uni-directional HV MOS devices.

Subfile: B C

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09/12/2002 [REDACTED]

8/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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6264450 INSPEC Abstract Number: B1999-07-2560R-028, C1999-07-7410D-054
Title: High-voltage MOS device modeling with BSIM3v3 SPICE model
Author(s): Myono, T.; Nishibe, E.; Kikuchi, S.; Iwatsu, K.;
Suzuki, T.; Sasaki, Y.; Itoh, K.; Kobayashi, H.
Author Affiliation: Sanyo Electr. Co. Ltd., Gunma, Japan
Journal: IEICE Transactions on Electronics Conference Title: IEICE Trans.
Electron. (Japan) vol.E82-C, no.4 p.630-7
Publisher: Inst. Electron. Inf. & Commun. Eng,
Publication Date: April 1999 Country of Publication: Japan
CODEN: IELEEEJ ISSN: 0916-8524
SICI: 0916-8524(199904)E82C:4L.630:HVDM;1-#
Material Identity Number: P712-1999-005
Conference Title: ICMTS 1998. Proceedings of 1998 International
Conference on Microelectronic Test Structures
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 23-26 March 1998 Conference Location: Kanazawa, Japan
Language: English
Abstract: This paper presents a new technique for modeling High-Voltage
lightly-doped-drain MOS (HV MOS) devices accurately with the BSIM3v3 SPICE
model. Standard SPICE models do not model the voltage dependency of R_s/ and R_d/ in HV MOS devices; this causes large discrepancies between
the simulated and measured I-V characteristics of HV MOS devices. We
propose to assign physical meanings and values different from the original
BSIM3v3 model to three of its parameters to represent the voltage
dependency of R_s/ and R_d. With this method, we have succeeded in
highly accurate parameter extraction, and the simulated I-V characteristics
of HV MOS devices, using the extracted parameters, match the measured
results well. The relationship between the proposed modeling technique and
the physical mechanism of HV MOS devices is also discussed based on
measurement and device simulation results. Since our method does not change
any model equations of BSIM3v3, it can be applied to any SPICE simulator on
which the BSIM3v3 model runs, so we can use SPICE simulation for accurate
circuit design of complex circuits using HV MOS devices.

Subfile: B C
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09/12/2002 0002-050

8/3,AB/5 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

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6036356 INSPEC Abstract Number: B9811-2560B-006, C9811-7410D-035

Title: Modelling technique for high-voltage MOS devices with BSIM3v3

Author(s): Myono, T.; Nishibe, E.; Iwatsu, K.; Kikuchi, S.;

Suzuki, T.; Sasaki, Y.; Itoh, K.; Kobayashi, H.

Author Affiliation: MOS-LSI Div., Sanyo Electr. Co. Ltd., Gunma, Japan

Journal: Electronics Letters vol.34, no.18 p.1790-1

Publisher: IEE,

Publication Date: 3 Sept. 1998 Country of Publication: UK

CODEN: ELLEAK ISSN: 0013-5194

SICI: 0013-5194(19980903)34:18L.1790:MTHV;1-3

Material Identity Number: E089-98018

U.S. Copyright Clearance Center Code: 0013-5194/98/\$10.00

Language: English

Abstract: A new technique is presented for modelling high-voltage (HV) MOS devices accurately with the BSIM3v3 SPICE model. Physical meanings different from those of the original BSIM3v3 are assigned to some parameters but without changing its model equations; this method can be applied to any SPICE simulator on which the BSIM3v3 model runs.

Subfile: B C

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09/12/2002 [REDACTED] 8

8/3,AB/6 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05435592

E.I. No: EIP99124941420
Title: High-voltage MOS device modeling with BSIM3v3 SPICE model
Author: Myono, Takao; Nishibe, Eiji; Kikuchi, Shuichi;
Iwatsu, Katsuhiko; Suzuki, Takuya; Sasaki, Yoshisato; Itoh, Kazuo;
Kobayashi, Haruo
Corporate Source: SANYO Electric Co Ltd, Gunma-ken, Jpn
Conference Title: Proceedings of the 1998 IEEE International Conference
on Microelectronic Test Structures (ICMTS)
Conference Location: Kanazawa, Jpn Conference Date: 19980523-19980526
E.I. Conference No.: 55697
Source: IEICE Transactions on Electronics v E82-C n 4 1999. p 630-637
Publication Year: 1999
CODEN: IELEEEJ ISSN: 0916-8524
Language: English

Abstract: This paper presents a new technique for modeling High-Voltage lightly-doped-drain MOS (HV MOS) devices accurately with the BSIM3v3 SPICE model. Standard SPICE models do not model the voltage dependency of R//s and R//d in HV MOS devices; this causes large discrepancies between the simulated and measured I-V characteristics of HV MOS devices. We propose to assign physical meanings and values different from the original BSIM3v3 model to three of its parameters to represent the voltage dependency of R//s and R//d. With this method, we have succeeded in highly accurate parameter extraction, and the simulated I-V characteristics of HV MOS devices using the extracted parameters match the measured results well. The relationship between the proposed modeling technique and the physical mechanism of HV MOS devices is also discussed based on measurement and device simulation results. Since our method does not change any model equations of BSIM3v3, it can be applied to any SPICE simulator on which the BSIM3v3 model runs, so we can use SPICE simulation for accurate circuit design of complex circuits using HV MOS devices. (Author abstract) 13 Refs.

09/12/2002 [REDACTED]

8/3,AB/7 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05359096

E.I. No: EIP99094782479
Title: Modeling and parameter extraction technique for high-voltage MOS device

Author: Myono, T.; Nishibe, E.; Kikuchi, S.; Iwatsu, K.;
Suzuki, T.; Sasaki, Y.; Itoh, K.; Kobayashi, H.
Corporate Source: SANYO Electric Co, Ltd, Osaka, Jpn
Conference Title: Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, ISCAS '99

Conference Location: Orlando, FL, USA Conference Date:
19990530-19990602

E.I. Conference No.: 55489
Source: Proceedings - IEEE International Symposium on Circuits and Systems v 6 1999. p VI-230-VI-233

Publication Year: 1999
CODEN: PICSDI ISSN: 0271-4310

Language: English
Abstract: This paper presents a novel technique for modeling HV MOS devices accurately with the BSIM3v3 SPICE model. We assign different meanings from the original BSIM3v3 to three parameters. The simulated I-V characteristics using the extracted parameters match the measured results well, and the physical mechanism of HV MOS devices is clarified based on device simulations. Since our method does not change any model equations of BSIM3v3, it can be applied to any on SPICE simulator on which the BSIM3v3 model runs. (Author abstract) 7 Refs.

09/12/2002 [REDACTED]

8/3,AB/8 (Item 3 from file: 8)
DIALOG(R) File 8:Ei Compendex(R)
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05343227

E.I. No: EIP99084761570
Title: Modelling technique for uni-directional HV MOS devices based on
BSIM3v3

Author: Myono, T.; Nishibe, E.; Kikuchi, S.; Iwatsu, K.;
Suzuki, T.; Sasaki, Y.; Itoh, K.; Kobayashi, H.

Corporate Source: SANYO Electric Co Ltd, Gunma, Jpn

Source: Electronics Letters v 35 n 14 1999. p 1200-1201

Publication Year: 1999

CODEN: ELLEAK ISSN: 0013-5194

Language: English

Abstract: A modeling technique for the uni-directional high-voltage metal-oxide **semiconductor** (HV MOS) is proposed. The proposed model uses a new parameter extraction technique. Simulated and measured results are given that confirm the accuracy of the proposed technique for modeling uni-directional HV MOS devices. 3 Refs.

09/12/2002 [REDACTED]

8/3,AB/9 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2002 Engineering Info. Inc. All rts. reserv.

05130907

E.I. No: EIP98104403769
Title: Modelling technique for high-voltage MOS devices with BSIM3v3
Author: Myono, T.; Nishibe, E.; Iwatsu, K.; Kikuchi, S.;
Suzuki, T.; Sasaki, Y.; Itoh, K.; Kobayashi, H.
Corporate Source: SANYO Electric Co Ltd, Gunma, Jpn
Source: Electronics Letters v 34 n 18 Sep 3 1998. p 1790-1791
Publication Year: 1998
CODEN: ELLEAK ISSN: 0013-5194
Language: English

Abstract: A new technique is presented for modelling high-voltage (HV) MOS devices accurately with the BSIM3v3 SPICE model. Physical meanings different from those of the original BSIM3v3 are assigned to some parameters but without changing its model equations; this method can be applied to any SPICE simulator on which the BSIM3v3 model runs. (Author abstract) 2 Refs.

09/12/2002 [REDACTED]

8/3, AB/10 (Item 1 from file: 94)
DIALOG(R) File 94: JICST-EPlus
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04755323 JICST ACCESSION NUMBER: 00A0402902 FILE SEGMENT: JICST-E
Modeling and Parameter Extraction Technique for Uni-Directional HV MOS
Devices.

MYONO T (1); NISHIBE E (1); KIKUCHI S (1); IWATSU K (1);
SUZUKI T (1); SASAKI Y (2); ITOH K (2); KOBAYASHI H (2)
(1) Sanyo Electric Co., Ltd., Gunma-ken, Jpn; (2) Gunma Univ.,
Kiryu-shi, Jpn

IEICE Trans Fundam Electron Commun Comput Sci (Inst Electron Inf Commun Eng),
2000, VOL.E83-A, NO.3, PAGE.412-420, FIG.13, TBL.1, REF.7

JOURNAL NUMBER: F0699CAT ISSN NO: 0916-8508

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: This paper presents a new technique for accurately modeling
uni-directional High-Voltage lightly-doped-drain MOS(HV MOS) devices by
extending the bi-directional HV MOS model and adopting a new parameter
extraction method. We have already reported on a SPICE model for
bi-directional HV MOS devices based on BSIM3v3. However, if we apply
this bi-directional HV MOS model and its parameter extraction technique
directly to uni-directional HV MOS devices, there are large
discrepancies between the measured and simulated I-V characteristics of
the uni-directional devices. This paper extends the bi-directional HV
MOS model, and adopts a new parameter extraction technique. Using
parameters extracted with the new method, the simulated I-V
characteristics of the uni-directional n-channel HV MOS device match
the measured results well. Since our method does not change any model
equations of BSIM3v3, it can be applied to any SPICE simulator on which
the BISM3v3 model runs. (author abst.)

09/12/2002 [REDACTED]

8/3, AB/11 (Item 2 from file: 94)
DIALOG(R) File 94: JICST-EPlus
(c) 2002 Japan Science and Tech Corp(JST). All rts. reserv.

03849762 JICST ACCESSION NUMBER: 99A0021838 FILE SEGMENT: JICST-E
High Voltage MOS Device Modeling with BSIM3v3 and its Parameter Extraction
Technique.

MYONO TAKAO (1); KIKUCHI SHUICHI (1); IWATSU KATSUHIKO (1);
NISHIBE EIJI (1); SUZUKI TAKUYA (1); SASAKI YOSHITOMO (2);
ITO KAZUO (2); KOBAYASHI HARUO (2)

(1) SANYO Electr. Co., Ltd.; (2) Gunma Univ., Fac. of Eng.

Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report
(Institute of Electronics, Information and Communication Engineers),
1998, VOL.98, NO.348(ED98 111-123), PAGE.79-86, FIG.10, TBL.1, REF.11

JOURNAL NUMBER: S0532BBG

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3 681.3:65.012.122

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: This paper presents a new technique for modeling High-Voltage(HV)
MOS devices accurately with the BSIM3v3 SPICE model. Standard SPICE
models do not model the voltage dependency of Rs and Rd in HV MOS
devices; this causes large discrepancies between the simulated and
measured I-V characteristics of HV MOS devices. We propose to assign
physical meanings and values different from the original BSIM3v3 model
to three of its parameters to represent the voltage dependency of Rs
and Rd. With this method, we have succeeded in highly accurate
parameter extraction and the simulated I-V characteristics of HV MOS
devices using the extracted parameters match the measured results well.
The relationship between the proposed modeling technique and the
physical mechanism of HV MOS devices is also discussed based on
measured and device simulation results. (author abst.)

09/12/2002 [REDACTED]

8/3,AB/12 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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03637278 JICST ACCESSION NUMBER: 98A0269817 FILE SEGMENT: JICST-E
Circuit Simulation Technique for High Voltage Level Shift Circuit Design.
MYONO TAKAO (1); IWATSU KATSUHIKO (1); KIKUCHI SHUICHI (1);

NISHIBE EIJI (1); SUZUKI TAKUYA (1)

(1) SANYO Electr. Co., Ltd.

Denki Gakkai Denshi Kairo Kenkyukai Shiryo, 1998, VOL.ECT-98, NO.11-18,
PAGE.43-48, FIG.18, TBL.1, REF.6

JOURNAL NUMBER: X0578AAN

UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Conference Proceeding

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

09/12/2002 00/002 058

8/3,AB/13 (Item 1 from file: 144)

DIALOG(R) File 144:Pascal

(c) 2002 INIST/CNRS. All rts. reserv.

14557264 PASCAL No.: 00-0223349

High-voltage MOS device modeling with BSIM3v3 SPICE model

MYONO T; NISHIBE E; KIKUCHI S; IWATSU K; SUZUKI T;

SASAKI Y; ITOH K; KOBAYASHI H

SANYO Electric Co Ltd, Gunma-ken, Japan

Proceedings of the 1998 IEEE International Conference on
Microelectronic Test Structures (ICMTS) (Kanazawa, Jpn)

1998-05-23/1998-05-26

Journal: IEICE Transactions on Electronics, 1999, v E82-C (4) 630-637

Language: English

This paper presents a new technique for modeling High-Voltage lightly-doped-drain MOS (HV MOS) devices accurately with the BSIM3v3 SPICE model. Standard SPICE models do not model the voltage dependency of Rs and Rd in HV MOS devices; this causes large discrepancies between the simulated and measured I-V characteristics of HV MOS devices. We propose to assign physical meanings and values different from the original BSIM3v3 model to three of its parameters to represent the voltage dependency of Rs and Rd. With this method, we have succeeded in highly accurate parameter extraction, and the simulated I-V characteristics of HV MOS devices using the extracted parameters match the measured results well. The relationship between the proposed modeling technique and the physical mechanism of HV MOS devices is also discussed based on measurement and device simulation results. Since our method does not change any model equations of BSIM3v3, it can be applied to any SPICE simulator on which the BSIM3v3 model runs, so we can use SPICE simulation for accurate circuit design of complex circuits using HV MOS devices.

09/12/2002 [REDACTED]

8/3,AB/14 (Item 2 from file: 144)
DIALOG(R) File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

14530919 PASCAL No.: 00-0195660
Modelling technique for uni-directional HV MOS devices based on BSIM3v3
MYONO T; NISHIBE E; KIKUCHI S; IWATSU K; SUZUKI T;
SASAKI Y; ITOH K; KOBAYASHI H
SANYO Electric Co Ltd, Gunma, Japan
Journal: Electronics Letters, 1999, 35 (14) 1200-1201
Language: English
A modeling technique for the uni-directional high-voltage metal-oxide semiconductor (HV MOS) is proposed. The proposed model uses a new parameter extraction technique. Simulated and measured results are given that confirm the accuracy of the proposed technique for modeling uni-directional HV MOS devices.

09/12/2002 [REDACTED]

8/3, AB/15 (Item 3 from file: 144)
DIALOG(R) File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

13693447 PASCAL No.: 98-0447686
Modelling technique for high-voltage MOS devices with BSIM3v3
MYONO T; NISHIBE E; IWATSU K; KIKUCHI S; SUZUKI T;
SASAKI Y; ITOH K; KOBAYASHI H
SANYO Electric Co Ltd, Gunma, Japan
Journal: Electronics Letters, 1998, 34 (18) 1790-1791
Language: English

A new technique is presented for modelling high-voltage (HV) MOS devices accurately with the BSIM3v3 SPICE model. Physical meanings different from those of the original BSIM3v3 are assigned to some parameters but without changing its model equations; this method can be applied to any SPICE simulator on which the BSIM3v3 model runs.

09/12/2002 [REDACTED]

12/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05579631
E.I. No: EIP00065194441
Title: Modeling and parameter extraction technique for uni-directional HV
MOS devices
Author: Myono, Takao; Nishibe, Eiji; Kikuchi, Shuichi;
Iwatsu, Katsuhiko; Suzuki, Takuya; Sasaki, Yoshisato; Itoh, Kazuo;
Kobayashi, Haruo
Corporate Source: SANYO Electric Co, Ltd, Gunma-ken, Jpn
Conference Title: 12th Workshop on Circuits and Systems
Conference Location: Karuizawa, Jpn Conference Date: 19990419-19990420
E.I. Conference No.: 56868
Source: IEICE Transactions on Fundamentals of Electronics, Communications
and Computer Sciences v E83-A n 3 Mar 2000. p 412-420
Publication Year: 2000
CODEN: IFESEX ISSN: 0916-8508
Language: English
Abstract: This paper presents a new technique for accurately modeling
uni-directional High-Voltage lightly-doped-drain MOS (HV MOS) devices by
extending the bi-directional HV MOS model and adopting a new parameter
extraction method. We have already reported on a SPICE model for
bi-directional HV MOS devices based on BSIM3v3. However, if we apply this
bi-directional HV MOS model and its parameter extraction technique directly
to uni-directional HV MOS devices, there are large discrepancies between
the measured and simulated I-V characteristics of the uni-directional
devices. This paper extends the bi-directional HV MOS model, and adopts a
new parameter extraction technique. Using parameters extracted with the new
method, the simulated I-V characteristics of the unidirectional n-channel
HV MOS device match the measured results well. Since our method does not
change any model equations of BSIM3v3, it can be applied to any SPICE
simulator on which the BSIM3v3 model runs. (Author abstract) 7 Refs.

12/3,AB/2 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

07940662 Genuine Article#: 226QM Number of References: 3
Title: Modelling technique for uni-directional HV MOS devices based on
BSIM3v3 (ABSTRACT AVAILABLE)
Author(s): Myono T (REPRINT) ; Nishibe E; Kikuchi S; Iwatsu K;
Suzuki T; Sasaki Y; Itoh K; Kobayashi H
Corporate Source: SANYO ELECT CO LTD, 1-1-1 SAKATA/GUNMA 3700596//JAPAN//
(REPRINT); GUNMA UNIV, DEPT ELECT ENGN/GUNMA 3768515//JAPAN//
Journal: ELECTRONICS LETTERS, 1999, V35, N14 (JUL 8), P1200-1201
ISSN: 0013-5194 Publication date: 19990708
Publisher: IEE-INST ELEC ENG, MICHAEL FARADAY HOUSE SIX HILLS WAY
STEVENAGE, HERTFORD SG1 2AY, ENGLAND
Language: English Document Type: ARTICLE
Abstract: A SPICE model for bi-directional AV MOS devices based on BSIM3v3
is extended by adopting a new parameter extraction method for modelling

09/12/2002

uni-directional HV MOS devices.

12/3,AB/3 (Item 2 from file: 34)
DIALOG(R) File 34:SciSearch(R) Cited Ref Sci
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07649692 Genuine Article#: 191RV Number of References: 13
Title: High-voltage MOS device modeling with BSIM3v3 SPICE model (ABSTRACT AVAILABLE)
Author(s): Myono T (REPRINT) ; Nishibe E; Kikuchi S; Iwatsu K;
 Suzuki T; Sasaki Y; Itoh K; Kobayashi H
Corporate Source: SANYO ELECT CO LTD,MOS LSI DIV/GUNMA//JAPAN/ (REPRINT);
 GUNMA UNIV,FAC ENGN, DEPT ELECT ENGN/KIRYU/GUMMA 3768515/JAPAN/
Journal: IEICE TRANSACTIONS ON ELECTRONICS, 1999, VE82C, N4 (APR), P630-637
ISSN: 0916-8524 Publication date: 19990400
Publisher: IEICE-INST ELECTRONICS INFORMATION COMMUNICATIONS ENG,
 KIKAI-SHINKO-KAIKAN BLDG MINATO-KU SHIBAKOEN 3 CHOME, TOKYO 105, JAPAN
Language: English Document Type: ARTICLE
Abstract: This paper presents a new technique for modeling High-Voltage
lightly-doped-drain MOS (HV MOS) devices accurately with the BSIM3v3
SPICE model. Standard SPICE models do not model the voltage dependency
of R-s and R-d in HV MOS devices; this causes large discrepancies
between the simulated and measured I-V characteristics of HV MOS
devices. We propose to assign physical meanings and values different
from the original BSIM3v3 model to three of its parameters to represent
the voltage dependency of R-s and R-d. With this method, we have
succeeded in highly accurate parameter extraction, and the simulated
I-V characteristics of HV MOS devices using the extracted parameters
match the measured results well. The relationship between the proposed
modeling technique and the physical mechanism of HV MOS devices is also
discussed based on measurement and device simulation results. Since our
method does not change any model equations of BSIM3v3, it can be applied
to any SPICE simulator on which the BSIM3v3 model runs, so we can
use SPICE simulation for accurate circuit design of complex circuits
using HV MOS devices.

12/3,AB/4 (Item 3 from file: 34)
DIALOG(R) File 34:SciSearch(R) Cited Ref Sci
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07079582 Genuine Article#: 122CP Number of References: 2
Title: Modelling technique for high-voltage MOS devices with BSIM3v3 (ABSTRACT AVAILABLE)
Author(s): Myono T (REPRINT) ; Nishibe E; Iwatsu K; Kikuchi S;
 Suzuki T; Sasaki Y; Itoh K; Kobayashi H
Corporate Source: SANYO ELECT CO LTD,MOS LSI DIV, 1-1-1 SAKATA/GUNMA
 3700596//JAPAN/ (REPRINT); GUNMA UNIV,DEPT ELECT ENGN/KIRYU/GUMMA
 3768515/JAPAN/
Journal: ELECTRONICS LETTERS, 1998, V34, N18 (SEP 3), P1790-1791
ISSN: 0013-5194 Publication date: 19980903
Publisher: IEE-INST ELEC ENG, MICHAEL FARADAY HOUSE SIX HILLS WAY
 STEVENAGE, HERTFORD SG1 2AY, ENGLAND

09/12/2002

Language: English Document Type: ARTICLE

Abstract: A new technique is presented for modelling high-holtage (HV) MOS devices accurately with the BSIM3v3 SPICE model. Physical meanings different from those of the original BSIM3v3 are assigned to some parameters but without changing its model equations: this method can be applied to any SPICE simulator on which the BSIM3v3 model runs.

09/12/2002 00/000 050

15/3, AB/1 (Item 1 from file: 94)
DIALOG(R) File 94:JICST-EPlus
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04623948 JICST ACCESSION NUMBER: 00A0297529 FILE SEGMENT: JICST-E
Performance Comparison of Drive Circuit for Switched Reluctance Motor.
SUZUKI TAKAHIRO (1); KIKUCHI SHINKI (1); WATANABE TADAALKI (2);
YANADA TOSHIAKI (2); ICHINOKURA OSAMU (2)

(1) Tohoku Gakuin Univ., Fac. of Eng.; (2) Tohoku Univ., Grad. Sch.
Tohoku Gakuin Daigaku Kogakubu Kenkyu Hokoku(Science and Engineering
Reports of Tohoku Gakuin University), 2000, VOL.34, NO.2, PAGE.63-66,
FIG.10, REF.14

JOURNAL NUMBER: S0937AAR ISSN NO: 0286-5904

UNIVERSAL DECIMAL CLASSIFICATION: 621.313.13

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: Switched reluctance motor(SRM) has desirable feature including simple construction, high reliability and low cost. However, it has some problems to solve such as large torque ripple and large noise. This paper describes performance comparison of drive circuits for SRM. A general circuit with SRM drive(Classic Circuit) and a split DC circuit(Split DC Circuit) are discussed based on the simulation and the experiments. The Split DC Circuit will realize low cost and compact drive system, because number of **semiconductor** devices are half of the Classic Circuit. It is confirmed that the motor performance with the Split DC Circuit higher than Classic Circuit. (author abst.)

09/12/2002 [REDACTED]

18/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

03429986 JICST ACCESSION NUMBER: 97A0772391 FILE SEGMENT: JICST-E
Assembly Technologies for Ball Grid Array.

TANIMOTO MITSUYOSHI (1); KANETA TOMONORI (1); **KIKUCHI SHIGERU** (2)
(1) Toshiba Corp., Prod. Div.; (2) Toshiba Corp., Ome Work.
Toshiba Rebyu(Toshiba Review), 1997, VOL.52,NO.8, PAGE.43-46, FIG.10,
TBL.1, REF.1

JOURNAL NUMBER: F0360AAK ISSN NO: 0372-0462 CODEN: TORBA

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: The ball grid array(BGA) mounting is used in electronic information devices such as personal computers and engineering workstations. The solder balls used for BGA connections are distributed over the bottom surface of the package. This allows the BGA to have a high pin count and small package size. Moreover, BGAs can be easily assembled with high yield using existing factory equipment. Toshiba has established various BGA assembly technologies, including electrode pad design and assembly process conditions. We have also studied the effect of alloy reactions on solder joint reliability.
(author abst.)

18/3,AB/2 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

01461340 JICST ACCESSION NUMBER: 92A0250407 FILE SEGMENT: JICST-E
A high-speed multichip switching module using a copper polyimide multilayer substrate.

OHSAKI T (1); KON T (1); SASAKI S (1); YAMANAKA N (2); **KIKUCHI S** (3)
(1) NTT Applied Electronics Lab., Tokyo, JPN; (2) NTT Transmission Systems Lab., Kanagawa, JPN; (3) NTT Communication Switching Lab., Tokyo, JPN

Denshi Tokyo(Denshi Tokyo), 1991, NO.29(1990), PAGE.163-166, FIG.9, REF.10

JOURNAL NUMBER: Y0773AAF ISSN NO: 0285-1903

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: A new high-speed multichip switching module for the B-ISDN(Broad-band Integrated Services Digital Network) is described. This module consists of 32 Si-bipolar LSIs and a multilayer polyimide dielectric substrate with a fine pattern of copper conductors. The 32*32 switching module can make 1:1 and 1:n connections at 1.8Gbps. (author abst.)

09/12/2002 00/00/00

20/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

04049339 JICST ACCESSION NUMBER: 99A0391971 FILE SEGMENT: JICST-E
Microelectronic Test Structures. High-Voltage MOS Device Modeling with
BSIM3v3 SPICE Model.

MYONO T (1); NISHIBE E (1); KIKUCHI S (1); IWATSU K (1); SUZUKI T (1)
; SASAKI Y (2); ITOH K (2); KOBAYASHI H (2)
(1) Sanyo Electric Co. Ltd., Gunma-ken, Jpn; (2) Gunma Univ., Kiryu-shi,
Jpn

IEICE Trans Electron(Inst Electron Inf Commun Eng), 1999, VOL.E82-C, NO.4,
PAGE.630-637, FIG.10, TBL.1, REF.13

JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: This paper presents a new technique for modeling **High**-Voltage lightly-doped-drain MOS (HV MOS) devices accurately with the BSIM3v3 SPICE model. Standard SPICE models do not model the voltage dependency of Rs and Rd in HV MOS devices; this causes large discrepancies between the simulated and measured I-V characteristics of HV MOS devices. We propose to assign physical meanings and values different from the original BSIM3v3 model to three of its parameters to represent the voltage dependency of Rs and Rd. With this method, we have succeeded in highly accurate parameter extraction, and the simulated I-V characteristics of HV MOS devices using the extracted parameters match the measured results well. The relationship between the proposed modeling technique and the physical mechanism of HV MOS devices is also discussed based on measurement and device simulation results. Since our method does not change any model equations of BSIM3v3, it can be applied to any SPICE simulator on which the BSIM3v3 model runs, so we can use SPICE simulation for accurate circuit design of complex circuits using HV MOS devices. (author abst.)

09/12/2002 09/002 058

22/3,AB/1 (Item 1 from file: 2)

DIALOG(R) File 2:INSPEC

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6979907 INSPEC Abstract Number: A2001-16-7970-012, B2001-08-2320-021

Title: Temperature dependence of field-emission characteristics from a p-type Si single emitter with real surface

Author(s): Yoshimoto, T.; Iwata, T.; **Kikuchi, S.**; Yokogawa, N.

Author Affiliation: Dept. of Inf. Sci., Hokkaido Univ., Sapporo, Japan

Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) vol.40, no.6A p.4197-8

Publisher: Japan Soc. Appl. Phys,

Publication Date: June 2001 Country of Publication: Japan

CODEN: JAPNDE ISSN: 0021-4922

SICI: 0021-4922(200106)40:6AL.4197:TDPE;1-S

Material Identity Number: F221-2001-013

Language: English

Abstract: The temperature dependence of field-emission current from a p-type Si single emitter with a real surface was investigated. The field emission pattern of the emitter did not show any symmetry which indicates a clean crystal structure of the surface; however, the highly nonlinear characteristics in $\log(I/V^{2/})$ vs. I/V plots (F-N plots) commonly observed from a clean p-type Si emitter are obtained. The emission current at the gentle slope region of F-N plots (I_{sat}) shows strong temperature dependence at a fixed applied voltage. The slope of $\log I_{sat}$ vs. $1/T$ plots gives an activation energy of 0.58 eV. The most probable conclusion is that the Fermi level is pinned at the middle of the band gap of the surface and electrons generated from the surface state to the conduction band are emitted.

Subfile: A B

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22/3,AB/2 (Item 2 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2002 Institution of Electrical Engineers. All rts. reserv.

5693171 INSPEC Abstract Number: A9720-8738-002, B9710-7230-141

Title: Construction of taste/odor recognition system using optimized sensory device

Author(s): Osada, H.; Yoshida, H.; Omamiuda, Y.; Ajishi, Y.; Seki, K.; **Kikuchi, S.**

Author Affiliation: Iwate Univ., Morioka, Japan

Journal: Transactions of the Institute of Electrical Engineers of Japan, Part E vol.117-E, no.7 p.371-6

Publisher: Inst. Electr. Eng. Japan,

Publication Date: July 1997 Country of Publication: Japan

CODEN: DGREF9 ISSN: 1341-8939

SICI: 1341-8939(199707)117:E:7L.371:CTOR;1-C

Material Identity Number: F143-97008

Language: Japanese

Abstract: With the improvement in the quality of life, food quality management has been increasingly required; however, taste and odor sensors

09/12/2002 [REDACTED]

for food evaluation were as yet undeveloped. We investigated a new taste/odor sensor utilizing the optimized sensory device (OSD), which is prepared by sintering a mixture of a magnetic **semiconductor** powder such as Mn-Zn ferrite and a ruthenium compound. When various taste and odor components of food adhere to the OSD, resistance or electromotive force based on surface electric **conduction** of the OSD change, and it therefore can clearly discriminate the type and quality of the foods. Moreover, the detected data are displayed as a pattern chart through computer processing. This paper describes preparation of a thick-film OSD and construction of the multi-channel taste/odor recognition system for some drinks.

Subfile: A B
Copyright 1997, IEE

22/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

03151487 INSPEC Abstract Number: B88037981, C88034891
Title: Cooling system for the FACOM M-780
Author(s): Yamamoto, H.; Nakata, M.; **Kikuchi, S.**
Author Affiliation: Fujitsu Ltd., Kawasaki, Japan
Journal: Fujitsu Scientific and Technical Journal vol.23, no.4 p.
243-54

Publication Date: Winter 1987 Country of Publication: Japan
CODEN: FUSTA4 ISSN: 0016-2523

Language: English
Abstract: The high operating speeds of large-scale mainframe computers have been achieved by reducing the speed-power product through **semiconductor** miniaturization and by increasing the numbers of circuits and improving system packaging density. The high operating speed and level of circuit integration of the FACOM M-780 have been enabled by developing a new type of cooling system. The **conductive** cooling module (CCM) used in this system makes use of a new cooling technology that allows LSI packages to generate much more heat and still perform reliably. Because individual processor-mounting boards can thus tolerate more heat, it becomes possible to build a high-performance single-board CPU. The article discusses the cooling system developed for the FACOM M-780.

Subfile: B C

22/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

00046680 INSPEC Abstract Number: A69030907, B69013336
Title: Preparation and properties of epitaxial gallium arsenide
Author(s): Maruyama, M.; **Kikuchi, S.**; Mizuno, O.
Author Affiliation: Nippon Electric Co., Ltd., Kawasaki, Japan
Journal: Journal of the Electrochemical Society vol.116, no.3 p.
413-15
Publication Date: March 1969 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

09/12/2002 09/902,958

Language: English

Abstract: High-purity epitaxial layers of n-type gallium arsenide have been grown by vapor deposition, using the reaction of arsenic trichloride with gallium. The purity of the layers was significantly increased when nominal 99.9999+% arsenic trichloride was substituted for nominal 99.999+% material. When the less-pure arsenic trichloride was used, there was a systematic variation in the electrical properties of layers grown in successive runs with the same gallium source. Resistivity and Hall coefficient measurements were made between 300 degrees and 4.2 degrees K. The maximum electron hall mobilities were 9180, 164000 and 175000 cm²/v-sec at 300 degrees , 77 degrees , 50 degrees K respectively. No impurity band conduction was observed even at 4.2 in pure samples.

Subfile: A B

22/3,AB/5 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

02202230 JICST ACCESSION NUMBER: 94A0850809 FILE SEGMENT: JICST-E
MCM for Server/Workstations.
FUKUNAGA NAOMI (1); SEYAMA KIYOTAKA (1); KIKUCHI SHUN'ICHI (1)
(1) Fujitsu Ltd.
SHM Kaishi (Journal of SHM (Society for Hybrid Microelectronics), 1994,
VOL.10,NO.5, PAGE.29-34, FIG.11, TBL.2, REF.3
JOURNAL NUMBER: S0579BBT ISSN NO: 0919-4398
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/12/2002 09/837,397

12sep02 13:26:10 User267149 Session D325.1

SYSTEM:OS - DIALOG OneSearch

File 348:EUROPEAN PATENTS 1978-2002/Sep W01

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File 349:PCT FULLTEXT 1983-2002/UB=20020905,UT=20020829

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STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

Set	Items	Description
S1	48988	SEMICONDUCT?????/TI,AB,CM
S2	6100	(GATE??(3N) (CONDUCT??? OR ELECTRODE? ? OR MICROELECTRODE? - ?))/TI,AB,CM
S3	197855	(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????)/TI,AB,CM
S4	30572	((ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????)(3N) (LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???))- /TI,AB,CM
S5	5391	((P OR N) ()TYPE? ?)/TI,AB,CM
S6	107439	(SUBSTRATE? ?)/TI,AB,CM
S7	29031	((INSULAT????? OR DIELECTRIC???) (3N) (LAYER??? OR FILM??? - OR COAT??? OR MULTILAYER??? OR SPACER???))/TI,AB,CM
S8	3632	((INSULAT????? OR DIELECTRIC???) (3N) GATE??)/TI,AB,CM
S9	9032	((LOW OR LOWER OR MIDDLE OR HIGH???) (3N) CONCENTRAT?????)/- TI,AB,CM
S10	513	((REVERSE?? OR BACKWARD) (3N) (ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????))/TI,AB,CM
S11	9375	((DRAIN???? OR SOURCE? ? OR CHANNEL???) (3N) (REGION???? OR - AREA????))/TI,AB,CM
S12	2209	((HIGH OR LOW OR LOWER) (3N) (DOPE???? OR DOPA???? OR DOPE???? OR DOPA????? OR DOPING OR IMPURIT?????))/TI,AB,CM
S13	3064	((DOPE???? OR DOPA???? OR DOPE???? OR DOPA????? OR DOPING OR IMPURIT?????)) (3N) CONCENTRAT?????)/TI,AB,CM
S14	3882	S1 AND S2
S15	3882	S14 AND S3
S16	1969	S15 AND S4
S17	461	S16 AND S5
S18	399	S17 AND S6
S19	310	S18 AND S7
S20	222	S19 AND S8
S21	59	S20 AND S9
S22	2	S21 AND S10
S23	57	S21 NOT S22
S24	47	S23 AND S11
S25	35	S24 AND S12
S26	35	S25 AND S13
S27	35	IDPAT (sorted in duplicate/non-duplicate order)
S28	35	IDPAT (primary/non-duplicate records only)
S29	0	S28 AND ((SUSTAIN???(3N) (VOLT???? OR POTENTIAL)))/TI,AB,CM
S30	22	S28 AND (VOLT????)/TI,AB,CM
S31	14	S30 AND (DRAIN????(2N) REGION???) /TI,AB,CM
S32	13	S31 AND (SOURCE???(2N) REGION???) /TI,AB,CM

22/TI,PD,PN,PY,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Conductivity-modulation metal oxide **semiconductor** field effect
transistor

MOS-Feldeffekt-Transistor mit Leitfähigkeitsmodulation

Transistor a effet de champ du type MOS a modulation de la conductivite

PATENT (CC, No, Kind, Date): EP 280535 A2 880831 (Basic)

EP 280535 A3 901010

EP 280535 B1 010718

Conductivity-modulation metal oxide **semiconductor** field effect
transistor

...ABSTRACT A2

A conductivity-modulation MOSFET employs a **substrate** (30) of an **N type** conductivity as its **N base**. A first source layer (34) of a heavily-doped **N type** conductivity is formed in a **P base** layer (32) formed in the **N base** (30). A source **electrode** (38) electrically **conducts** the **P base** (32) and the source (34). A first **gate electrode** (36) **insulatively** covers a channel region (CH1) defined by the **N⁺** source layer (34) in the **P base** (32). A **P drain layer** (44) is formed on an opposite **substrate** surface. An **N⁺** second source layer (46) is formed in a **P type** drain layer (44) by diffusion to define a second channel region (CH2). A second **gate electrode** (40) **insulatively** covers the second channel region (CH2), thus providing a voltage-controlled turn-off controlling transistor. A drain **electrode** (48) of the MOSFET **conducts** the **P type** drain (44) and second source (46). When the turn-off controlling transistor is rendered **conductive** to turn off the MOSFET a "shorted anode structure" is temporarily formed wherein the **N type** base (30) is short-circuited to the drain **electrode** (48), whereby case, the flow of carriers accumulated in the **N type** base (30) into the drain **electrode** is facilitated to accelerate dispersion of carriers upon turn-off of the transistor. ...

9. A conductivity-modulation unipolar field effect transistor device comprising a **semiconductive substrate** (30, 30('), 50, 80, 100, 200); a first **semiconductive base layer** (30, 30('), 50, 80, 106, 106('), 222) of a first conductivity type provided in said **substrate**; a first **semiconductive diffusion layer** (32, 84, 204) of a second conductivity type formed in said **substrate** and serving as a second base of said device; a second **semiconductive diffusion layer** (34, 88, 208) of the first conductivity type formed in said first diffusion layer and serving as a first source of said device, said second diffusion layer defining said a first channel region (CH1) in said first diffusion layer ; a source **electrode layer** (38, 68, 92, 212), formed on said **substrate**, for electrically connecting said first and second diffusion layers; and a first **gate electrode layer** (36, 36('), 96, 216), insulatively provided above said **substrate**, for covering said first channel region,

characterized in that said device further comprises a third **semiconductive diffusion layer** (44, 86, 206) of the second conductivity type formed in said **substrate** and serving as a drain of said device; a fourth **semiconductive diffusion layer** (46, 90, 210) of the first conductivity type formed in said third diffusion layer and serving as a second source of said device, said fourth diffusion layer defining a second channel region (CH2) in said third diffusion layer; a drain **electrode layer** (48, 72, 94, 214, 242), formed on said **substrate**, for electrically connecting said third and fourth diffusion layers; and a second **gate electrode layer** (40, 62, 98, 218), insulatively provided above said **substrate**, for covering said second channel region, said fourth diffusion layer and said second **gate electrode layer** constituting a voltage-controlled switching transistor which is rendered **conductive** when said device is turned off, and temporarily forms a "shorted anode structure" in said device, thereby increasing an electrical connectivity between said first base **layer** and said drain **electrode layer**, so as to facilitate carriers accumulated in said first base layer to flow into said drain **electrode layer**, whereby dispersion of carriers in said device is accelerated to increase a turn-off speed thereof.

10. The device according to claim 9, characterized in said drain **electrode layer** (48, 72, 94, 214, 242).

11. The device according to claim 10, characterized in that when said switching transistor is rendered **conductive**, a **reverse-conducting diode** consisting of said first and second base layers is formed, said **reverse-conducting diode** being **reverse-biased** when said device is turned off, thereby increasing a withstand voltage of said device.

12. The device according to claim 11, characterized in that said device further comprises a **semiconductive buffer layer** (42, 82, 104, 220) of the first conductivity type formed in said **substrate** and connected to said third diffusion layer, said buffer layer suppressing generation of a punch-through phenomenon to increase a withstand voltage of said device and to decrease a forward voltage drop of said **reverse-conducting diode**.

13. The device according to claim 10, characterized in that said device further comprises a heavily-doped diffusion layer (52, 234) of the second...

32/TI, PD, PN, PY, K/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Field effect **semiconductor** device
Feldeffekt-Halbleiterbauelement
Dispositif **semiconducteur** a effet de champ
PATENT (CC, No, Kind, Date): EP 1102327 A2 010523 (Basic)

...ABSTRACT A2

A HDTMOS includes a Si **substrate**, a buried oxide film and a **semiconductor** layer. The **semiconductor** layer includes an upper Si film, an epitaxially grown Si buffer layer, an epitaxially grown SiGe film, and an epitaxially grown Si film. Furthermore, the HDTMOS includes an **n-type high concentration** Si body region, an **n-** Si region, a SiGe channel region containing **n-type low concentration impurities**, an **n-type low concentration** Si cap layer, and a contact which is a **conductor member** for electrically connecting the **gate electrode** and the Si body region. The present invention extends the operation range while keeping the threshold **voltage** small by using, for the channel layer, a material having a smaller potential at the band edge where carriers travel than that of a material...

1. A **semiconductor** device comprising:

a **substrate**;
a **semiconductor** layer provided in a part of the **substrate**;
a **gate insulator film** provided on the **semiconductor layer**;
a **gate electrode** provided on the **gate insulator film**;
source and drain regions of a first conductivity type provided in regions on both sides of the **gate electrode** of the **semiconductor layer**;
a channel region made of a first **semiconductor** provided in a **region** between the source and drain regions of the **semiconductor layer**;
a body region made of a second **semiconductor** of a second conductivity type having a larger potential for carriers at a band edge where carriers travel than that of the first **semiconductor**, provided in a **region** below the **channel region** of the **semiconductor layer**; and
a **conductor member** for electrically connecting the **gate electrode** and the **body region**.

2. The **semiconductor** device according to claim 1, further comprising a cap layer made of a **semiconductor** having a larger potential for carriers at a band edge where carriers travel than that of the first **semiconductor**, provided in a **region** between the **channel region** and the **gate insulator film** of the **semiconductor layer**.

3. The **semiconductor** device according to claim 1,

wherein at least an uppermost portion of the **substrate** is

constituted by an insulator.

4. The **semiconductor** device according to claim 1,

wherein the **channel region** contains **impurities** in a lower concentration than that of the **body region** by 1/10 or less.

5. The **semiconductor** device according to claim 1,
9. The **semiconductor** device according to claim 7,

wherein the **source and drain regions** are **p-type source and drain regions**,
the **channel region** is a **channel region for p-channel**, and
the **body region** is an **n-type body region**.

10. The **semiconductor** device according to claim 7,

wherein the **source and drain regions** are **n-type source and drain regions**,
the **channel region** is a **channel region for n-channel**, and
the **body region** is a **p-type body region**.

11. The **semiconductor** device according to claim 9, comprising:
another **semiconductor** layer provided on the **substrate**;
another **gate insulator film** provided on the other **semiconductor layer**;
another **gate electrode** provided on the other **gate insulator film**;
n-type source and drain regions provided in regions on both sides of the other **gate electrode** of the other **semiconductor layer**;
a **channel region for n-channel** containing Si and Ge as constituent elements, and provided in a region between the **n-type source and drain regions** of the other **semiconductor layer**;
a **p-type body region** made of Si provided in a **region below the channel region for n-channel** of the other **semiconductor layer**; and
another **conductor member** for electrically connecting the other **gate electrode** and the **p-type body region**, wherein the **semiconductor** device functions as a complementary type device.

12. The **semiconductor** device according to claim 1,

21. The **semiconductor** device according to claim 18,

wherein the **source and drain regions** are **n-type source and drain regions**,
the **channel region** is a **channel region for n-channel**, and
the **body region** is a **p-type body region**.

22. The **semiconductor** device according to claim 20, comprising:
another **semiconductor** layer provided on the **substrate**;
another **gate insulator film** provided on the other **semiconductor layer**;
another **gate electrode** provided on the other **gate**

insulator film;
n-type source and drain regions provided
in regions on both sides of the other gate
electrode of the other semiconductor layer;
a channel region for n-channel containing Si, Ge and C
as constituent elements, provided in a region between the n-
type source and drain regions of the other
semiconductor layer;
a p-type body region made of Si, provided in a region
below the channel region of the other semiconductor
layer; and
another conductor member for electrically connecting the other
gate electrode and the p-type body region,
wherein the semiconductor device functions as a complementary
type device.

32/TI,PD,PN,PY,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor device and method of manufacturing the same
Halbleiteranordnung und Herstellungsverfahren
Dispositif **semiconducteur** et son procédé de fabrication
PATENT (CC, No, Kind, Date): EP 852401 A2 980708 (Basic)
EP 852401 A3 981111

...ABSTRACT A2

A **semiconductor substrate** made of **P-type** silicon is formed with two MOS transistors having a first **gate electrode** and a second **gate electrode** placed in parallel with each other. A first **N-type** impurity drain diffusion layer and a second **N-type** impurity source diffusion layer are connected in series between the first and second **gate electrodes**. A first **high-concentration P-type impurity** diffusion layer for threshold control is formed in a source-side portion of a **channel region** of the **semiconductor substrate** underlying a portion of the first **gate electrode** closer to the first **N-type impurity** source diffusion layer, while a second **high-concentration P-type impurity** diffusion layer for threshold control is formed under a portion of the second **gate electrode** closer to the second **N-type impurity** source diffusion layer.

CLAIMS 1. A **semiconductor device** comprising:

a single **semiconductor substrate**; and
a plurality of MIS transistors formed on said **semiconductor substrate**, one of said MIS transistors of a first conductivity type having a **source region** connected in series to a **drain region** of another of said MIS transistors of the first conductivity type,

said MIS transistors having respective **gate electrodes** placed in parallel with each other on said **semiconductor substrate** and respective **channel regions** formed in said **semiconductor substrate** to underlie said individual **gate electrodes** such that carriers drift in the same direction in each of said **channel regions**,
a concentration of an **impurity** of a second conductivity type being higher in a portion of each of said **channel regions** closer to said **source region** than in a portion of each of said **channel regions** closer to said **drain region**.

2. A **semiconductor device** comprising:

a single **semiconductor substrate**; and
a NAND circuit formed on said **semiconductor substrate**, said NAND circuit being composed of two P-channel MOS transistors each having **source** and **drain regions** connected in parallel to **source** and **drain regions** of the other

P-channel MOS transistor, respectively, and of two N-channel MOS transistors each having a **source region** connected in series to a **drain region** of the other N-channel MOS transistor,

said two N-channel MOS transistors having respective **gate electrodes** placed in parallel with each other on said **semiconductor substrate** and respective **channel regions** formed in said **semiconductor substrate** to underlie said individual **gate electrodes** such that carriers drift in the same direction in each of said **channel regions**, a concentration of a **p-type** impurity being higher in a portion of each of said **channel regions** closer to said **source region** than in a portion of each of said **channel regions** closer to said **drain region**.

3. A **semiconductor device** comprising:

a single **semiconductor substrate**; and
a NOR circuit formed on said **semiconductor substrate**, said NOR circuit being composed of two P-channel MOS transistors each having a **source region** connected in series to a **drain region** of the other P-channel MOS transistor and of two N-channel MOS transistors each having **source** and **drain regions** connected in parallel to **source** and **drain regions** of the other N-channel MOS transistor, respectively,

said MIS transistors of the first conductivity type having respective **gate electrodes** placed in parallel with each other on said **semiconductor substrate** and respective **channel regions** of the first conductivity type formed in said **semiconductor substrate** to underlie said individual **gate electrodes** such that carriers drift in the same direction in each of said **channel regions** of the first conductivity type,

a **concentration** of an **impurity** of the second conductivity type being higher in a portion of each of said **channel regions** of the first conductivity type closer to said **source region** than in a portion of each of said **channel regions** of the first conductivity type closer to said **drain region**,

said MIS transistors of the second conductivity type having respective **gate electrodes** placed in parallel with each other on said **semiconductor substrate**; and respective **channel regions** of the second conductivity type formed in said **semiconductor substrate** to underlie said individual **gate electrodes** such that carriers drift in the same direction in each of said **channel regions** of the second conductivity type,

a **concentration** of an **impurity** of the first conductivity type being higher in a portion of each of said **channel regions** of the second conductivity type closer to said **source region** than in a portion of each of said **channel regions** of the second conductivity type closer to

said drain region.

said N-channel MOS transistors composing said NAND circuit having respective gate electrodes placed in parallel with each other on said semiconductor substrate and respective N-type channel regions formed in said semiconductor substrate to underlie said individual gate electrodes such that carriers drift in the same direction in each of said N-type channel regions,

a concentration of a P-type impurity being higher in a portion of each of said N-type channel regions closer to said source region than in a portion of each of said N-type channel regions closer to said drain region,

said P-channel MOS transistors composing said NOR circuit having

respective gate electrodes placed in parallel with each other on said semiconductor substrate and respective P-type channel regions formed in said semiconductor substrate to underlie said individual gate electrodes such that carriers drift in the same direction in each of said P-type channel regions,

a concentration of an N-type impurity being higher in a portion of each of said P-type channel regions closer to said source region than in a portion of each of said P-type channel regions closer to said drain region.

9. A semiconductor device comprising:

a single semiconductor substrate; and

a plurality of MIS transistors of a first conductivity type formed on said semiconductor substrate, said MIS transistors of the first conductivity type having respective gate electrodes placed in parallel with each other and respective source and drain regions formed at both ends of respective lengths of said gate electrodes,

a channel region being formed under the gate electrode of one of said MIS transistor

32/TI,PD,PN,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Equipment for communication system and **semiconductor** integrated circuit device
Ausstattung eines Kommunikationssystems und integrierter Halbleiterschaltkreisbauelement
Equipement d'un systeme de communication et dispositif de circuit integre semi-conducteur
PATENT (CC, No, Kind, Date): EP 1209740 A2 020529 (Basic)

...ABSTRACT A2

Equipment for a communication system has a **semiconductor** device formed by integrating a Schottky diode, a MOSFET, a capacitor, and an inductor in a SiC **substrate**. The SiC **substrate** has a first multilayer portion and a second multilayer portion provided upwardly in this order. The first multilayer portion is composed of (delta)-doped layers each containing an **n-type impurity** (nitrogen) at a **high concentration** and undoped layers which are alternately stacked. The second multilayer portion is composed of (delta) - doped layers each containing a **p-type impurity** (aluminum) at a **high concentration** and undoped layers which are alternately stacked. Carriers in the (delta) -doped layers spread out extensively to the undoped layers. Because of a **low impurity concentration** in each of the undoped layers, scattering by impurity ions is reduced so that a low resistance and a high breakdown voltage are obtained.

...CLAIMS A2

1. Equipment for a communication system disposed in the communication system and having an active element formed by using a compound **semiconductor**, the active element comprising:
a compound **semiconductor** layer provided on a **substrate**; and
an active region provided on the compound **semiconductor** layer and composed of at least one first **semiconductor** layer functioning as a carrier flow region and at least one second **semiconductor** layer containing an impurity for carriers at a **high concentration** and smaller in film thickness than the first **semiconductor** layer such that the carriers are distributed therein under a quantum effect, the first and second **semiconductor** layers being disposed in contact with each other.
2. The equipment for a communication system of claim 1, wherein the first **semiconductor** layer includes a plurality of first **semiconductor** layers and the second **semiconductor** layer includes a plurality of second **semiconductor** layers, the first **semiconductor** layers and the second **semiconductor** layers being arranged in stacked relation.
3. The equipment for a communication system of claim 1, wherein the active element is a MESFET formed by disposing the first **semiconductor** layer immediately below a **gate electrode**.

4. The equipment for a communication system of claim 1, wherein the active element is a Schottky diode formed by disposing the first **semiconductor** layer immediately below a Schottky **electrode**.
5. The equipment for a communication system of claim 4, wherein the active element is the Schottky diode in a lateral configuration.
6. The equipment for a communication system of claim 1, wherein the active element is a MISFET comprising:
a **gate insulating film** provided on the first **semiconductor layer**;
a **gate electrode** provided on the **gate insulating film**; and
source/drain regions provided on both sides of the **gate electrode** in the compound **semiconductor** layer.
7. The equipment for a communication system of claim 1, further having a capacitor and an inductor provided on the compound **semiconductor** layer.
8. The equipment for a communication system of claim 1, wherein the compound **semiconductor** layer is a SiC layer.
9. The equipment for a communication system of claim 1, which is a base station in the communication system.
18. The **semiconductor** integrated circuit device of claim 13, wherein the active element is a MISFET comprising:
a **gate insulating film** provided on the first **semiconductor layer**;
a **gate electrode** provided on the **gate insulating film**; and
source/drain regions provided on both sides of the **gate electrode** in the compound **semiconductor** layer.

22/TI,PD,PN,PY,K/1 (Item 1 from file: 348)
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Photoelectric conversion **semiconductor** device
Photoelektrische Halbleiter-Umwandlungsvorrichtung
Dispositif semi-conducteur de conversion photoélectrique
PATENT (CC, No, Kind, Date): EP 718896 A2 960626 (Basic)
EP 718896 A3 970910

Photoelectric conversion **semiconductor** device
Dispositif semi-conducteur de conversion photoélectrique

...ABSTRACT A2

Photoelectric conversion **semiconductor** device having very little reverse bias leakage. A **P+** type impurity region (3) and a guard ring (17) formed on one surface of an **N** type **semiconductor substrate** (1) and an **N⁺ type** impurity region (4) formed on the opposite surface. On the **P⁺ type** impurity region a gate SiO₂(sub(2)) (5), a gate Si₃N₄(sub(4)) (6), an upper portion SiO₂(sub(2)) (7) and...

...3)N(sub(4)), upper portion SiO₂(sub(2)) and gate polysilicon being formed in the same shape. A bias voltage is applied by a **reverse** voltage applying **electrode** (13) via a polysilicon resistor (9) and capacity readout is performed by a readout **electrode** (11). (see image in original document)

A photoelectric conversion **semiconductor** device comprising:

a first conductivity type **semiconductor substrate** (1),
a second conductivity type impurity region (3) on a surface of the first conductivity type **semiconductor substrate**,
a gate SiO₂(sub(2)) (5) on the second conductivity type impurity region,
a dielectric layer (6, 7) on the gate SiO₂(sub(2)), and
a gate electrode (8) on the dielectric layer,
and characterised in that the dielectric layer is formed in the same shape as the gate electrode.

2. A photoelectric conversion **semiconductor** device as claimed in claim 1, wherein the dielectric layer is a gate Si₃N₄(sub(4)) (6) and an upper portion SiO₂(sub(2)) (7) on the gate Si₃N₄(sub(4)).
3. A photoelectric conversion **semiconductor** device as claimed in claim 1 or claim 2, wherein a first conductivity type impurity region (4) having an impurity concentration higher than the impurity concentration of the substrate is formed on a surface opposite the surface on which the second conductivity type impurity region is formed, a gate SiO₂(sub(2)), dielectric layer and gate electrode are sequentially formed on the first conductivity type impurity region, and said dielectric layer is formed in the same shape as said gate electrode
9. A method of fabricating a photoelectric conversion **semiconductor** device comprising the steps of:
forming a second conductivity type impurity region (3) on one surface

of a first conductivity type **semiconductor substrate** (1);
forming a gate SiO₂ (5) on the second conductivity type impurity region;
forming a **dielectric layer** (6, 7) on the gate SiO₂ (5);
forming a **gate electrode** (8) on the **dielectric layer**; and
forming a **reverse voltage applying electrode** (13) in the second conductivity type impurity region, and a resistor element (9) is formed connected to the **reverse voltage applying electrode**, characterised in that the **gate electrode** and resistor element are formed from the same polysilicon film.

10. A photoelectric conversion **semiconductor** device comprising:
a second conductivity type impurity region (3) on one surface of a first conductivity type **semiconductor substrate** (1);
a first conductivity type impurity region (4) having an impurity concentration higher than the **substrate** formed on an opposite surface to the surface on which the second conductivity type impurity region is formed;

32/TI,PD,PN,PY,K/4 (Item 4 from file: 348)
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Semiconductor device and method for fabricating the same
Halbleiteranordnung und Verfahren zur Herstellung
Dispositif semi-conducteur et son procede de fabrication
PATENT (CC, No, Kind, Date): EP 820096 A2 980121 (Basic)
EP 820096 A3 000830

...CLAIMS the adjacent shallow well region.

2. A semiconductor device comprising:

a semiconductor substrate;
a deep well region of a first conductivity type formed in the **semiconductor substrate**, which is capable of functioning as an emitter or a collector of a bipolar transistor;
a shallow well region of a second conductivity type formed in the deep well region, which is capable of functioning as a base of the bipolar transistor;
a **source region** and a **drain region** of the first conductivity type, formed in the shallow well region, which are capable of functioning as the collector or the emitter of the bipolar transistor;
a **channel region** formed between the **source region** and the **drain region**;
a **gate insulating film** formed on the **channel region**; and
a **gate electrode** formed on the **gate insulating film**,

wherein the **gate electrode** is electrically connected to the shallow well region, and

the **semiconductor device** is operated by a combination of an operation of a MOS transistor and an operation of the bipolar transistor.

6. A **semiconductor device** according to claim 1, wherein the **gate electrode** includes a polycrystalline silicon film formed on the **gate insulating film** and a metal silicide film formed on the polycrystalline silicon film, and wherein the metal silicide film is electrically connected to the shallow well region via the contact region of the shallow well region, a **high concentration impurity diffusion region**, in which an impurity of the same conductivity type as that of the shallow well region is diffused at a **higher concentration** than that of a remainder of the shallow well region, is formed in the contact region, and an Ohmic contact is formed between the metal silicide film and the shallow well region through the **high concentration impurity diffusion region**.

7. A **semiconductor device** according to claim 2, wherein the **gate electrode** includes a polycrystalline silicon film formed on the **gate insulating film** and a metal silicide film formed on the polycrystalline silicon film, and wherein the metal silicide film is electrically connected to the shallow well region via the contact region of the shallow well region,

- a **high concentration impurity** diffusion region, in which an impurity of the same conductivity type as that of the shallow well region is diffused at a **higher concentration** than that of a remainder of the shallow well region, is formed in the contact region, and
 - an Ohmic contact is formed between the metal silicide film and the shallow well region through the **high concentration impurity** diffusion region.
8. A **semiconductor** device according to claim 1, further comprising an interlayer **insulating film** and an upper wiring provided on the interlayer **insulating film**, wherein a contact hole is formed in the interlayer **insulating film**, which penetrates through the **gate electrode** and the **gate insulating film** so as to reach the contact region of the shallow well region, wherein a **high concentration impurity** diffusion region, in which an impurity of the same conductivity type as that of the shallow well region is diffused at a **higher concentration** than that of a remainder of the shallow well region, is formed in the contact region, an Ohmic contact is formed between the upper wiring and the shallow well region through the **high concentration impurity** diffusion region on the bottom of the contact hole, and wherein an Ohmic contact is formed between the **gate electrode** and the upper wiring on a side wall region of the contact hole.
10. A method for fabricating a **semiconductor** device comprising:
- a **semiconductor substrate**;
 - a deep well region of a first conductivity type, formed in the **semiconductor substrate**;
 - a plurality of shallow well regions of a second conductivity type, formed in the deep well **region**;
 - a **source region** and a **drain region** of the first conductivity type, respectively formed in the plurality of shallow well **regions**;
 - a **channel region** formed between the **source region** and the **drain region**;
 - a **gate insulating film** formed on the **channel region**; and
 - a **gate electrode** formed on the **gate insulating film**,
- wherein the **gate electrode** is electrically connected to corresponding one of the shallow well regions, and the shallow well region is electrically separated from the adjacent shallow well region,
- wherein the P-channel MOS transistor includes a **p-type source region** and a **p-type drain region** formed in the shallow **n-type well region**, a **channel region** formed between the **p-type source region** and the **p-type drain region**, a **gate insulating film** formed on the **channel region**, and a **p-type gate electrode** formed on the **gate insulating film**.

09/12/2002 09/837,397

film, and
wherein the **n-type gate electrode** is
electrically connected to the shallow **p-type** well region,
and the **p-type gate electrode** is electrically
connected to the shallow **n-type** region.

32/TI, PD, PN, PY, K/5 (Item 5 from file: 348)
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LD MOSFET or MOSFET with an integrated circuit containing thereof and manufacturing method
LD-MOSFET oder MOSFET mit einer diese enthaltenden integrierten Schaltung und Verfahren zur Herstellung
LD MOSFET ou MOSFET avec un circuit integre contenant celui-ci et methode de fabrication
PATENT (CC, No, Kind, Date): EP 789401 A2 970813 (Basic)
EP 789401 A3 980916

...ABSTRACT A2

In forming a P-) body diffused layer in a portion on the source side of an N-) drain diffused layer of a DMOSFET, **P-type** impurity ions are implanted at a large tilt angle to reach a part of a region underlying an N+) **gate electrode** by using, as a mask, a resist film having an opening corresponding to a region in which the body diffused layer of the DMOSFET is to be formed and the N+) **gate electrode** so as to be activated. Thereafter, an N+) source diffused layer and an N+) drain diffused layer are formed in the P-) body diffused layer and in the N-)drain diffused layer, respectively. Since a high-temperature drive-in process need not be performed to introduce the **P-type** impurity ions into the region underlying the N+) **gate electrode**, a reduction or variations in threshold **voltage** and the degradation of a gate oxide film each caused by the impurity diffused from the N+) **gate electrode** can be prevented. Consequently, there is provided a **semiconductor** device having a DMOSFET mounted thereon which has a reduced on-resistance and suppresses the activation of a parasitic bipolar transistor due to reduced variations in threshold **voltage** and a high-quality gate oxide film.

CLAIMS 1. A **semiconductor** device having at least one DMISFET mounted in an active region of a **semiconductor substrate** surrounded by an isolation, wherein

 said DMISFET comprises:
 a first impurity diffused layer formed by introducing an impurity of first conductivity type or impurity of second conductivity type at a low concentration into said active region;
 a gate insulating film formed on said active region;
 a gate electrode formed on said gate insulating film;
 a source diffused layer formed by introducing the impurity of first conductivity type at a high concentration into a portion of said active region located on one side of said gate electrode;
 a drain diffused layer formed by introducing the impurity of first conductivity type at a high concentration into a portion of said active region located on the other side of said gate electrode to be surrounded by said first impurity diffused layer; and

- a second impurity diffused layer formed by introducing the impurity of second conductivity type on a concentration level for threshold control into a portion surrounding said source diffused layer and reaching a part of an area underlying said **gate electrode** in said active region, said second impurity diffused layer being apart from said drain diffused layer with intervention of said first impurity diffused layer.
 - a **gate insulating film** formed on said second active region;
 - a **gate electrode** formed on said **gate insulating film**; and
 - source/drain diffused layers formed by introducing the impurity of first conductivity type into respective areas located on both sides of said **gate electrode** in said second active region and said second MISFET comprises:
 - a **gate insulating film** formed on said third active region;
 - a **gate electrode** formed on said **gate insulating film**; and
 - source/drain diffused layers formed by introducing the impurity of second conductivity type into respective areas located on both sides of said **gate electrode** in said third active region.
9. A **semiconductor** device according to claim 8, wherein the **gate insulating films** of said first and second MISFETs are composed of the same material as that composing the **gate insulating film** of said DMISFET and have the same thickness as that of the **gate insulating film** of said DMISFET and the **gate electrodes** of said first and second MISFETs are composed of the same material as that composing the **gate electrode** of said DMISFET and have the same thickness as that of the **gate electrode** of said DMISFET.
10. A **semiconductor** device having at least one DMISFET mounted in an active region of a **semiconductor substrate** surrounded by an isolation, wherein
- said DMISFET comprises:
 - a first impurity diffused layer formed by introducing an impurity of first conductivity type or impurity of second conductivity type at a low concentration into said active region;
 - a **gate insulating film** formed on said active region;
 - a **gate electrode** formed on said **gate insulating film**;
 - insulator sidewalls formed on both side faces of said **gate electrode**
 - a source diffused layer formed by introducing the impurity of first conductivity type at a high concentration into a portion of said active region located on one side of said **gate electrode** and having the position of an edge thereof closer to the **gate electrode** determined by said insulator sidewalls;
 - a drain diffused layer formed by introducing the impurity of first conductivity type at a high concentration into a portion of said active region located on the other side of said **gate electrode** to be surrounded by said first impurity diffused

- layer; and
a second impurity diffused layer formed by introducing the impurity of second conductivity type on a concentration level for threshold control into a portion of said active **region** surrounding said **source** diffused layer and reaching a part of an area underlying said **gate electrode** and having an edge thereof closer to the **gate electrode** determined by the edge on the source side of said **gate electrode**.
11. A **semiconductor** device according to claim 10, wherein
said second impurity diffused layer has such a profile that a depth of penetration in said **semiconductor substrate** becomes larger at a portion closer to the center thereof in a portion of said active **region** underlying the **source** diffused layer.
12. A **semiconductor** device according to claim 10, wherein said DMISFET further comprises
a third impurity diffused layer formed by introducing the impurity of first conductivity type at a **high concentration** into an area of said active region including a deep portion of said second impurity diffused layer and not including the vicinity of a surface thereof.
13. A **semiconductor** device according to claim 10, further comprising
a first MISFET having a first-conductivity-type channel structure formed in a second active region of said **semiconductor substrate** surrounded by said isolation a thickness as that of the **gate electrode** of said DMISFET.
15. A **semiconductor** device according to claim 13, wherein low-concentration source/drain diffused layers are formed by introducing an **impurity** at a **lower concentration** than and of the same conductivity type as the impurity introduced into the source/drain diffused layers of said MISFET between an area underlying said **gate electrode** and said source/drain diffused layers in at least one of said second and third active regions.
16. A **semiconductor** device having at least one MISFET for high voltage mounted in an active region of a **semiconductor substrate** surrounded by an isolation, wherein
said MISFET for high **voltage** comprises:
a **gate insulating film** formed on said active region;
a **gate electrode** formed on said **gate insulating film**;

32/TI,PD,PN,PY,K/6 (Item 6 from file: 348)
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Thin film transistor in insulated semiconductor substrate and manufacturing method thereof

Dunnfilmtransistor über einem isolierten Halbleitersubstrat und Verfahren zur Herstellung

Transistor a couche mince sur un substrat semi-conducteur isole et methode de fabrication

PATENT (CC, No, Kind, Date): EP 749165 A2 961218 (Basic)
EP 749165 A3 970924
EP 749165 B1 010926

1. A **semiconductor device**, comprising:
a **semiconductor substrate** of a first conductivity type having a first **impurity concentration**;
an **insulating layer** formed on said **semiconductor substrate**;
a **semiconductor layer** formed on said **insulating layer**, said **semiconductor layer** including a region of a second conductivity type;
a **gate insulating film** selectively formed on said **semiconductor layer**;
a **gate electrode** formed on said **gate insulating film**; and
first and second sidewalls respectively formed on sides of said **gate electrode**; wherein said **semiconductor layer** is defined as a **channel formation region** under said **gate insulating film**, defined as first and second additional **semiconductor regions** of the second conductivity type under said first and second sidewalls, and defined as first and second **semiconductor regions** of the second conductivity type in regions adjacent to said first and second additional **semiconductor regions**, respectively, on sides opposite to said **channel formation region**, and a predetermined **voltage** is applied to said **gate electrode** to cause a current to flow between said first **semiconductor region** and said second **semiconductor region** through said **channel formation region**; and
wherein said **semiconductor substrate** includes a **high concentration** region of the first conductivity type and having a second **impurity concentration higher than** said first **impurity concentration**, said **high concentration** region being formed extending from under said **channel formation region** to under respective said first and second **semiconductor regions**, said **high concentration** region being formed in a surface of said **semiconductor substrate** under said **channel formation region**, and in a region at a predetermined depth from the surface of said **semiconductor substrate** under respective said first and second **semiconductor regions**.
2. The **semiconductor device** according to claim 1, wherein said **gate electrode** comprises,

a first partial **gate electrode** formed on said **gate insulating film**, and
a second partial **gate electrode** formed on said first partial **gate electrode**, and
at least one of said first and second partial **gate electrodes** is formed of a refractory metal.

3. A **semiconductor device**, comprising:

a **semiconductor substrate** of a first conductivity type having a first **impurity concentration**;
an **insulating layer** formed on said **semiconductor substrate**;
a **semiconductor layer** formed on said **insulating layer**, said **semiconductor layer** including a region of a second conductivity type;
a **gate insulating film** selectively formed on said **semiconductor layer**;
a **gate electrode** formed on said **gate insulating film**; and
first and second sidewalls respectively formed on sides of said **gate electrode**; wherein said **semiconductor layer** is defined as a **channel formation region** under said **gate insulating film**, defined as first and second additional **semiconductor regions** of the second conductivity type under said first and second sidewalls, and defined as first and second **semiconductor regions** of the second conductivity type in regions adjacent to said first and second additional **semiconductor regions**, respectively, on sides opposite to said **channel formation region**, and a predetermined **voltage** is applied to said **gate electrode** to cause a current to flow between said first **semiconductor region** and said second **semiconductor region** through said **channel formation region**; and

wherein said **semiconductor substrate** includes a high **concentration** region of the first conductivity type having a second **impurity concentration higher than** said first **impurity concentration**, said high **concentration** region being formed in a surface of said **semiconductor substrate** from under said **channel formation region** to under parts of respective said first and second additional **semiconductor regions**.

4. A **semiconductor device** comprising a first transistor of a second conductivity type formed on a first **semiconductor substrate** of a first conductivity type and having a first **impurity concentration** and a second transistor of the first conductivity type formed on a second **semiconductor substrate** of the second conductivity type and having a second **impurity concentration**, wherein

said first transistor comprises,
said first **semiconductor substrate**,
a first **insulating layer** formed on said first **semiconductor substrate**,
a first **semiconductor layer** formed on said first

insulating layer, said first semiconductor layer including a region of the second conductivity type, a first gate insulating film selectively formed on said first semiconductor layer, a first gate electrode formed on said first gate insulating film, and first and second sidewalls formed on sides of said first gate electrode, respectively, wherein said first semiconductor layer is defined as a first channel formation region under said first gate insulating film, defined as first and second additional semiconductor regions of the second conductivity type under said first and second sidewalls, and defined as first and second semiconductor regions of the second conductivity type in regions adjacent to said first and second additional semiconductor regions, respectively, on sides opposite to said first channel formation region, and a predetermined voltage is applied to said first gate electrode to cause a current to flow between said first semiconductor region and said second semiconductor region through said channel formation region; and

wherein said first semiconductor substrate includes a first high concentration region of the first conductivity type and having a third impurity concentration higher than said first impurity concentration, said first high concentration region being formed extending from under said first channel formation region to under said first and second semiconductor regions, said first high concentration region being formed in a surface of said first semiconductor substrate under said first channel formation region, and in a region at a predetermined depth from the surface of said first semiconductor substrate under respective said first and second semiconductor regions

- (d) forming a resist on said conductive layer and patterning the resist into a predetermined form;
- (e) performing an etching process to said conductive layer using said resist as a mask, remaining said conductive layer and said insulating film being defined as a gate electrode and a gate insulating film, respectively, said semiconductor layer being defined as a channel formation region in a region under said gate electrode and being defined as electrode regions in other region;
- (f) implanting impurities of said first conductivity type with predetermined implantation energy from above to form a high concentration region having a second impurity concentration higher than said first impurity concentration in said semiconductor substrate, said high concentration region being formed from under said channel formation region to under said electrode regions, said high concentration region being formed in a surface of said semiconductor substrate under said channel formation region, and in a region at a

32/TI,PD,PN,PY,K/7 (Item 7 from file: 348)
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High **voltage** integrated circuit, high **voltage** junction
terminating structure, and high **voltage** MIS transistor
Integrierter Hochspannungsschaltkreis, Hochspannungsübergangsabschlussstruk-
tur und MIS-Hochspannungstransistor
Circuit integre a haute tension, structure terminale de jonction a haute
tension et transistor MIS a haute tension
PATENT (CC, No, Kind, Date): EP 738011 A2 961016 (Basic)
EP 738011 A3 990506

..ABSTRACT A2

A high **voltage** integrated circuit is provided that includes a
first region (1) of first conductivity type; a second region (2) of
second conductivity type formed in a...

...surface of the first region; a third region (3) of first conductivity
type formed in a selected area of a surface layer of the second
region (2); a first **source region** (11) and a first
drain region (11) of the first conductivity type formed in
the second region (2) remote from the third region (3); a first
gate electrode (15) formed on a surface of the second region
(2) between the first **source region** (11) and first
drain region (11), through an **insulating film**
(13); second **source region** (12) and second **drain**
region (12) of second conductivity type formed in a surface layer
of the third region (3); and a second **gate electrode** (15)
formed on a surface of the third region (3) between the second
source region (12) and the second **drain region**
(12), through an **insulating film** (13). (see image in
original document) ...

..CLAIMS A2

1. A high **voltage** integrated circuit comprising:
a first region of first conductivity type;
a second region of second conductivity type formed in a selected area
of a first major surface of the first region;
a third region of first conductivity type formed in a selected area
of a surface of the second **region**;
first **source region** and first **drain region** of
the first conductivity type formed in selected areas of the surface
of the second region remote from the third region;
a first **gate electrode** formed on a surface of the second
region between the first **source region** and the
first **drain region**, through an **insulating**
film;
second **source region** and second **drain region**
of second conductivity type formed in selected areas of a surface of
the third region; and
a second **gate electrode** formed on a surface of the third
region between the second **source region** and the
second **drain region**, through an **insulating**

film.

2. A high **voltage** integrated circuit as defined in claim 1, wherein the second region is formed such that an edge of a depletion layer appearing in the second...

...2), the net doping amount being obtained by subtracting a doping amount of first-conductivity-type impurities from a doping amount of second-conductivity-type **impurities** region, the fourth region being surrounded by the second region.

6. A high **voltage** integrated circuit as defined in claim 5, further comprising a first **conductive film** formed on a surface of the first region interposed between the second region and the fourth region, through an **insulating film**, such that the first **conductive film** partially overlaps the second and fourth regions.
13. A high **voltage** integrated circuit as defined in claim 9, which is integrated with an n-channel vertical power device on the same **semiconductor substrate**, the first region being formed in common with an **n-type** layer of **low impurity concentration**, including an **n-type** drift layer or a **low concentration n-type** drain layer, of the n-channel vertical power device.
18. A high **voltage** integrated circuit as defined in claim 1, further comprising at least one fifth region of second conductivity type in a selected area of the surface of the second region adjacent to the third region, the at least one fifth region having a **higher impurity concentration** than the second region.
21. A high **voltage** integrated circuit as defined in claim 18, wherein the second region includes an active region in which is formed a MOSFET comprising the first **source region** and first **drain region** formed in the surface layer of the second region, and the first **gate electrode** formed on the surface of the second **region** between the first **source region** and the first **drain region**, the fifth **region** being formed in a major part of the surface of the second region excluding the active region.
25. A high **voltage** junction terminating structure as defined in claim 24, further comprising an **insulating film** on the ninth region, a second **conductive film** at least partially overlapping the **insulating film**, a third **conductive film** at least partially overlapping the **insulating film**, and a high resistance film contacting the second and third **conductive films** and covering the **insulating film** between the second and third **conductive films**.

the second-conductivity-type-channel high **voltage MIS** transistor comprises: the high **voltage** junction terminating structure; a first drain **electrode** disposed on one side of the high **voltage** junction terminating structure, such that the first drain **electrode** is electrically connected to the eighth region; a base region of first conductivity type formed on the other

side of the high **voltage** junction terminating structure, such that the base region is in contact with the ninth **region**; a **source region** of second conductivity type formed in a selected area of a surface of the base **region**; a **channel region** of second conductivity type located in the surface of the base region interposed between the eighth **region** and the **source region** of second conductivity type; a first **gate insulating film** formed on the **channel region** of second conductivity type; a third **gate electrode** formed on the first **gate insulating film**; and a first source **electrode** electrically connected to at least the **source region** of second conductivity type.

a first-conductivity-type-channel MIS transistor comprising first **source region** and first **drain region** of first conductivity type formed in selected areas of the surface of the second region remote from the third region, and a first **gate electrode** formed through an **insulating film** on a surface of the second region interposed between the first **source region** and the first **drain region**;

a second-conductivity-type-channel MIS transistor comprising second **source region** and second **drain region** of second conductivity type formed in selected areas of the surface of the third region, and a second **gate electrode** formed through an **insulating film** on a surface of the third region interposed between the second **source region** and the second **drain region**.

32/TI,PD,PN,PY,K/8 (Item 8 from file: 348)
DIALOG(R) File 348: (c) 2002 European Patent Office. All rts. reserv.

Vertical type **semiconductor** device.

Halbleiterbauelement vom vertikalen Typ.

Dispositif a semi-conducteur du type vertical.

PATENT (CC, No, Kind, Date): EP 477873 A2 920401 (Basic)
EP 477873 A3 930331
EP 477873 B1 951115

A vertical type **semiconductor** device capable of greatly decreasing the on-resistance without impairing the breakdown **voltage** of the element. In the fundamental DMOS cells 2 that control the current to constitute the vertical **semiconductor** device, through hole cells 3 are arranged along the sides of the cell that form a channel 21. The through hole cell 3 has a through hole 23 extending from the surface of an n^(sup -)-type drift region toward an n^(sup +)-type **drain region** 12, and has an n^(sup +)-type through hole region 25 that is formed by diffusing impurities from the inner wall of the through hole 23 and that is continuous to the n^(sup +)-type **drain region** 12. A breakdown **voltage** of the element is maintained by the n^(sup -)-type drift region 11 between a p-type well region 13 and the n^(sup +)-type through hole region 25 or the n^(sup +)-type **drain region** 12. Owing to the disposition of the through hole cells 3, the JFET resistance component becomes negligibly small between the DMOS cells 2 neighboring along...

...CLAIMS A3

1. A vertical type **semiconductor** device wherein a **semiconductor substrate** of a first type of conduction consists of a **layer** of a **high impurity concentration** and a **layer** of a **low impurity concentration**, the **layer** of said **high impurity concentration** serves as a **drain region**, the **surface** of the **layer** of said **low impurity concentration** forms a **main surface**, a **well region** of a second type of conduction is formed in a portion of said **main surface**, a **source region** of the first type of conduction is formed in a portion of the **surface** of said **well region**, a **gate electrode** is formed on a periphery of said **well region** of the second type of conduction via an **insulating film** in order to form a **channel region** on the periphery of said **well region**, the **layer** of said **low impurity concentration** forms a **drift region** between said **well region** of the second type of conduction and said **drain region**, and a current between the **drain** and the **source** is controlled by applying a **voltage** to said **gate electrode**, and wherein a **hole** is formed extending from said **main surface** between said neighboring **well regions** up to said **drain region** passing through the **layer** of said **low impurity concentration** (**drift region**), and the electric resistance in the lengthwise direction of said **hole** is set to be smaller than the electric resistance of the **layer** of said **low impurity concentration** inside or around said

hole.

a current control cell region that controls the current between the drain and the source and is comprised of a well region of a second type of **conduction** that is connected to one region of said **semiconductor** layer buried in the surface of said **semiconductor** layer, and has a PN junction relative to said **semiconductor** layer, the PN junction terminating in the surface of said **semiconductor** layer; a **source region** of the first type of **conduction** having a PN junction relative to said well region, the PN junction terminating in the surface of said well region; and an **insulated gate** structure constituted on a **channel region** that consists of the surface of said well region between the drift **region** and the **source region**

18. A vertical type **semiconductor** device comprising:

a first **semiconductor** layer constituted by a **semiconductor** layer of a first type of **conduction** that forms a **drain region**;

a second **semiconductor** layer of the first type of **conduction** that is formed on the main surface of said first **semiconductor** layer and has an **impurity concentration lower than the impurity concentration of said drain region**;

32/TI,PD,PN,PY,K/9 (Item 9 from file: 348)
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Insulated-gate type integrated circuit
Integrierte Schaltung mit isoliertem Gate
Circuit integre du type a grille isolee
PATENT (CC, No, Kind, Date): EP 441390 A2 910814 (Basic)
EP 441390 A3 911227
EP 441390 B1 980826

...ABSTRACT A2

A P-well region (11) is provided in a **semiconductor substrate** (10) of **N-type**. A P-channel MOSFET is arranged in the **N-type substrate** (10) while an N-channel MOSFET is arranged in the P-well **region** (11). The **drain regions** (14, 15) of their respective MOSFETs consist of **high concentration impurity diffused regions** (21, 23) and **low concentration impurity diffused regions** (22, 24) arranged about their respective **high concentration impurity diffused regions**. Also, a **drain electrode** (17) is provided to cover at above the entire of the **high and low concentration impurity diffused regions** (21, 23, 22, 24). (see image in original document)

CLAIMS 1. An **insulated-gate type integrated circuit** including a **high voltage insulated-gate type field effect transistor**, comprising:
a **gate electrode** (17);
a **drain region** (14, 15) arranged in the surface area of a **first semiconductor region** (10, 11) of a **first conductive type**, said **drain region** consisting of a **low concentration impurity diffused region** (22, 24) of a **second conductive type** provided at one side of, and adjacent to, said **gate electrode** and a **high concentration impurity diffused region** (21, 23) of said **second conductive type** provided next to said **low concentration impurity diffused region**;
a **source region** (13, 16) arranged in the surface area of said **first semiconductor region**, said **source region** (13, 16) being at a distance from said **drain region** and consisting of at least a **high concentration impurity diffused region** of said **second conductive type**;
said **gate electrode** (17) being arranged on the surface area of said **first semiconductor region** and interposed between said **source region** and said **low concentration impurity diffused region** of said **drain region**;
;
an **insulating layer** (20) arranged to cover the entire arrangement including said **gate electrode**; and
a **conductor layer** (19) connected electrically via an aperture provided in said **insulating layer** to said **drain region** and arranged on said **insulating**

- layer to extend above said **drain reg**
- 2. An **insulated-gate** type integrated circuit according to claim 1, characterised in that both of said **low** and **high concentration impurity** diffused regions (24, 23) of said **drain region** (15) are arranged within a **P-type** well region (11).
 - 4. An **insulated-gate** type integrated circuit according to claim 3, characterised in that said **low concentration impurity** diffused region (22, 24) is provided about said **high concentration impurity** diffused region (21, 23).
 - 5. An **insulated-gate** type integrated circuit according to claim 1, 3 or 4, characterised in that a higher **voltage** than a common supply **voltage** is applied to said **drain region**.
 - 6. An **insulated-gate** type integrated circuit according to claim 1, 3 or 4, characterised in that both of said **low** and **high concentration impurity** diffused **regions** of said **drain region** are of **N-t**

32/TI,PD,PN,PY,K/10 (Item 10 from file: 348)
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Semiconductor integrated circuit device and the method of manufacturing the same.

Integrierte Halbleiterschaltungsanordnung und Verfahren zu ihrer Herstellung.

Dispositif de circuit integre semi-conducteur et son procede de fabrication.

PATENT (CC, No, Kind, Date): EP 427255 A2 910515 (Basic)
EP 427255 A3 910904

In a **semiconductor** integrated circuit device comprising a bipolar transistor (NPN), complementary **insulated gate** type transistors (NMOS, PMOS), and a charge coupled device (CCD) formed in a single **semiconductor** chip (1, 3), a **semiconductor** substrate region of one (NMOS) of the complementary **insulated gate** type transistors (NMOS, PMOS) and a **semiconductor** substrate region of the charge coupled device (CCD) are formed in an epitaxial layer (3) without separation from each other. Thus, even when a low power source **voltage** (e.g., 5 V) is used, circuit characteristic (increase of the linearity of the operational amplifier of the output circuit, expansion of the dynamic range...).

...CLAIMS A3

1. A **semiconductor** integrated circuit device comprising a bipolar transistor (NPN), complementary **insulated gate** transistors (NMOS, PMOS), and a charge coupled device (CCD) formed in a single **semiconductor** chip (1, 3), characterized in that a **semiconductor** substrate region of one (NMOS) of said complementary **insulated gate** type transistors and a **semiconductor** substrate region of said charge coupled device (CCD) are formed in an epitaxial layer (3) without separating from each other.
2. The **semiconductor** integrated circuit characterized by comprising:
a **P-type** **semiconductor** body (1, 3) comprising a **semiconductor** substrate (1) having an epitaxially grown **P-type** epitaxial layer (3) formed on said **substrate**;
;
N-type buried layers (21, 22) which are selectively formed inside of said **semiconductor** body;
N-well regions (41, 42) which are respectively formed in a **P-channel** MOS transistor (PMOS) forming region and an NPN bipolar transistor forming region both in a surface region of said **semiconductor** body; and
a **semiconductor** substrate region of an **N-channel** MOS transistor (NMOS) and a **semiconductor** substrate region of a charge coupled device (CCD) respectively formed in said **P-type** epitaxial layer without separating from each other.
3. A method of manufacturing a **semiconductor** integrated circuit characterized by comprising the steps of:
selectively forming, inside of a **semiconductor**

substrate (1), buried layers (21, 22) having a **high impurity concentration** and of a conductivity type opposite to that of said **substrate**, and forming an epitaxial layer (3) of the same conductivity type as that of said **substrate** on a surface of said **substrate**

4. The method of manufacturing a semiconductor integrated circuit characterized by comprising the steps of:

selectively forming, inside of a **P-type** silicon **substrate** (1), N^(sup +) buried layers (21, 22) of a **high N-type impurity concentration**, and forming a **P-type** epitaxial layer (3) on a surface of said **substrate**;

selectively forming first and second N-well regions (41, 42) in said **P-type** epitaxial layer so that said first and second N-well regions are respectively connected to said N^(sup +) buried layers;

forming an internal base region (20) of an NPN transistor in said second N-well **region** and a buried **channel** of said charge coupled device in said **P-type** epitaxial layer;

forming a second gate oxide film (13) on the surface of said **first-layer electrode**;

forming a **second-layer electrode** (14) of said charge coupled device;

forming a **drain region** (161(sub 1)) and a **source region** (161(sub 2)) of said N-channel MOS transistor, a charge input region (162(sub 1)) and a charge output region (162(sub 2)) of said charge coupled device, a **drain region** (181(sub 1)) and a **source region** (1812) of said P-channel MOS transistor, and the external base region (182) of said NPN transistor;

32/TI,PD,PN,PY,K/11 (Item 1 from file: 349)
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SEMICONDUCTOR POWER DEVICE MANUFACTURE
FABRICATION D'UN SEMICONDUCTEUR DE PUISSANCE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200003427 A1 20000120 (WO 0003427)
Publication Year: 2000

English Abstract

In the manufacture of a **semiconductor** power device such as a trench-gate power MOSFET, a **source region** (13) is formed using a sidewall extension (30) of an upstanding **insulated-gate** structure (11, 21, 22). The sidewall extension (30) forms a step with an adjacent surface area (10a') of a body region (15) of a first conductivity type and comprises doped **semiconductor** material (13a) of opposite, second conductivity type which is separated from the **gate** (11) by **insulating** material (22). The body **region** (15) provides a **channel-accommodating** portion (15a) adjacent to the **gate structure** (11, 21, 22) and also comprises a localised **high-doped** portion (15b) which extends to a greater depth in the **semiconductor** body (10) than the shallow p-n junction between the **source region** (13) and the **channel-accommodating** portion (15a), and preferably deeper even than the bottom of the trench (20) of a trench-gate device. This **high-doped** portion (15b) is formed by introducing dopant of the first conductivity type into the **semiconductor** body (10) via the stepped-down adjacent surface area (10a') while using the stepped-up sidewall extension (30) comprising the doped **source region** material (13a) to mask the underlying **channel area**. **Source electrode** material (33) is deposited over the step so as to contact the doped **semiconductor** material (13a) of the sidewall extension (30) and the adjacent surface area (10a') of the **high-doped** portion (

In the transistor cell areas of this device, a **channel-accommodating** portion 15a of a body region 15 of a first conductivity type (i.e. **p-type** in this example) separates **source** and **drain regions** 13 and 14, respectively, of an opposite second conductivity type (**n-type** in this example). The gate 11 is present in a trench 20 which extends through 10 the regions 13 and 15 into an underlying portion of the **drain region** 14. The application of a **voltage** signal to the gate 11 in the on-state of the device serves in known manner for inducing a **conduction channel** 12 in the **region** portion 15a and for controlling current flow in this **conduction channel** 12 between the **source** and **drain regions** 13 depositing **electrode** material for the **source electrode** 33 over the step so as to contact the doped **semiconductor** material 13a of the sidewall 5 extension 30 and the adjacent surface area 10a' of the first conductivity type (Figure 10). It is the **high-doped** portion 15b of the body region 15 that is contacted by the **source electrode** 33 at the said adjacent surface area 10a'. This **high-doped** portion 15b has a **doping concentration** (P+) of the first

conductivity type which is higher than that (P) of the channel-accommodating portion 15a but lower than the conductivity-determining **dopant concentration** (N++) of the doped semiconductor material 13a of the sidewall extension 30 that provides the **source region** 13. The **high-doped** portion 15b is provided to a greater depth in the **semiconductor** body 10 than the p-n junction 18 between the **source region** 13 and the **channel**-accommodating portion 15a of the body region 15, and is preferably even deeper (as illustrated in Figures 7 to 10) than the p-n junction 19a between the channel-accommodating portion 15a and the underlying **drain region** body surface 10a (Figure 6). The height of the doped sidewall extension 30 (**source region** material 13a) which is retained above the surface 10a may be, for example, 0.5pm to 1.5pm This arrangement permits the realisation of a device with a very shallow depth for the p-n junction 18 between the **source region** 13 and the channel-accommodating portion 15a, while using doped **semiconductor** material 13a of 5 high conductivity in the step so as to avoid a high resistance in this shallow **source region** 13. Thus, the device can be made with a short channel length 12 and so with a low on-resistance between the **source** and **drain regions** 13 and

32/TI,PD,PN,PY,K/12 (Item 2 from file: 349)
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ANGLED LATERAL POCKET IMPLANTS ON P-TYPE SEMICONDUCTOR
DEVICES
IMPLANTATIONS LATÉRALES INCLINEES EN CASES SUR DES DISPOSITIFS SEMI-
CONDUCTEURS DU TYPE P
Patent and Priority Information (Country, Number, Date):
Patent: WO 9527306 A1 19951012
Publication Year: 1995

English Abstract

The punchthrough capacity of a **p-type semiconductor** device is significantly improved by nonuniformly doping the p-channel with **n-type** implants such as phosphorus. The **n-type** dopants are implanted at large angles to form pocket implants within the **channel region**. The dose of the implants, angle of the implants and the thermal cycle annealing of the implants will be optimized for maximum punchthrough capability without substantially detracting from the performance of the **semiconductor** device

A method for nonuniformly doping a **channel region** in a **p-type MOSFET** comprising the steps of:

(A) providing an **n-type semiconductor substrate**;
(B) forming a **gate insulating film** on said **substrate**;
(C) forming a **conductive layer** upon said **gate insulating film** and which forms the **gate electrode**;
(D) doping the entire **source and drain regions** of said **substrate** with a **p-type** dopant to a **first impurity concentration** which is self aligned to the **gate electrode**;
(E) doping said **substrate** with an **n-type** dopant to form first and second pockets containing **n-type** dopant and having a **second impurity concentration** that is **lower** than said **first impurity concentration**, wherein said **n-type** dopant is implanted at an angle greater than 00 from a line drawn perpendicular to the surface of said **substrate** and wherein said first pocket is beneath the **gate insulating layer** and adjacent to the **source region** and said second pocket is beneath the **gate insulating layer** and adjacent to the **drain region**;

and
(F) thermally treating said **substrate** to electrically activate said dopants.

2e The method of according to any preceding claim, wherein said **n-type** dopant is arsenic or phosphorus.

3e The method according to any preceding claim,

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wherein said **p-type** dopant is boron.

4* The method according to any preceding claim,
wherein the steps of doping with the **p-type** dopant and
doping with the **n-type** dopant are effected in order to
reduce punchthrough susceptibility of the **p-type** MOSFET
and wherein the **p-type** MOSFET has a threshold voltage
of about @0.5 to 9 Ve

5* The method according to any preceding claim,
wherein said **p-type** dopant is implanted at a dosage
greater than about 10¹⁶ atoms/cm²,

10@ 6e The method according to any preceding claim,
wherein said **p-type** dopant is implanted at a dosage
greater than about 10¹⁷ atoms/cm²,

7* The method according to any preceding claim,
wherein said first **impurity concentration** ranges from
about 10¹¹
10²¹ atoms/cm³.

32/TI,PD,PN,PY,K/13 (Item 3 from file: 349)
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HIGH SATURATION CURRENT, LOW LEAKAGE CURRENT FERMI THRESHOLD FIELD EFFECT
TRANSISTOR

TRANSISTOR A EFFET DE CHAMP A SEUIL DE FERMI, A COURANT DE SATURATION ELEVE
ET A COURANT DE FUITE FAIBLE

Patent and Priority Information (Country, Number, Date):

Patent: WO 9419830 A1 19940901

Publication Year: 1994

A high saturation current, low leakage, Fermi threshold field effect transistor includes a predetermined minimum **doping concentration** of the source and drain facing the channel to maximize the saturation current of the transistor. Source and **drain** doping gradient **regions** between the **source/drain** and the channel, respectively, of thickness greater than 300 Å are also provided. The threshold **voltage** of the Fermi-FET may also be lowered from twice the Fermi potential of the **substrate**, while still maintaining zero static electric field in the channel perpendicular to the **substrate**, by increasing the **doping concentration** of the channel from that which produces a threshold **voltage** of twice the Fermi potential. By maintaining a predetermined channel depth, preferably about 600 Å, the saturation current and threshold **voltage** may be independently varied by increasing the source/drain **doping concentration** facing the channel and by increasing the excess carrier concentration in the channel, respectively. A Fermi-FET having a **gate insulator** thickness of less than 120 Å, and a channel length of less than about 1 μm can thereby provide a P-channel saturation current of from said **substrate** surface, at least said channel depth being selected to produce zero static electric field perpendicular to said **substrate** surface at said **substrate** surface.

82 The P-channel field effect transistor of
Claim 81 further comprising a **P-type** tub region in said
semiconductor region at said **substrate** surface,
surrounding said **source region**, said **drain region**
and
said **channel region**, and extending a second depth from
said **substrate** surface which is greater than said
channel depth, at least said channel depth and said
second depth being selected to produce zero static
electric field perpendicular to said **substrate** surface
from said **substrate** surface to said channel depth.

83 An N-channel field effect transistor
comprising:
a **P-type semiconductor substrate**;
spaced apart **N-type source** and **drain**
regions
in said **semiconductor substrate** at a surface thereof;
an **N-type** channel in said **semiconductor**
substrate between said spaced apart **source** and **drain**

regions, said N-type channel being less than about one micron long; a gate insulating layer on said substrate surface, between said spaced apart source and drain regions, said gate insulating layer being less than about one hundred twenty Angstroms thick; and source, drain and gate electrodes, contacting said source and drain regions and said gate insulating layer, respectively, said source, drain and gate electrodes applying voltages to said source, drain and gate insulating layer respectively, of magnitude between about zero and five volts, to produce a drain saturation current in said field effect transistor of at least seven Amperes per centimeter of channel width and a leakage current...

A field effect transistor comprising:
a semiconductor substrate having a first doping concentration of first conductivity type;
a tub region having a second doping concentration of second conductivity type in said substrate at a surface thereof, and extending a first depth from said substrate surface;
spaced apart source and drain regions of said second conductivity type in said tub region at said substrate surface;
a channel of said second conductivity type in said tub region, between said spaced apart source and drain regions, and extending a second depth from said substrate surface, wherein said second depth is less than said first depth, and wherein said first doping concentration is greater than said second doping concentration;
a gate insulating layer on said substrate surface, between said spaced apart source and drain regions; and source, drain and gate electrodes contacting said source and drain regions and said gate insulating layer, respectively
a source doping gradient region of said second conductivity type between said source region and said channel, and being doped at a doping gradient which decreases from said first doping concentration adjacent said source region to said second doping concentration adjacent said channel, said source doping gradient region having thickness greater than 300 Angstroms;
a gate insulating layer on said substrate surface, between said spaced apart source and drain regions; and

**source, drain and gate electrodes contacting
said source and drain regions and said gate
insulating
layer, respectively.**

90 The field effect transistor of Claim 89
further comprising:
a **drain doping gradient region** of said second
conductivity type between said **drain region** and said
channel, and being doped at a doping gradient which
decreases from said first **doping concentration** adjacent
said **drain region** to said second **doping
concentration**
adjacent said channel, said **drain doping gradient
region** having thickness greater than 300 Angstroms.

91 The field effect transistor of Claim 89
wherein said **gate insulating layer** and said **gate
electrodes** extend over said **source** doping gradient
region.

92 The field effect transistor of Claim 91
wherein said **gate insulating layer** and said **gate
electrode** extend over said **drain doping gradient
region**.

93 The field effect transistor of Claim 89
wherein said **source** doping gradient **region** surrounds
said **source region**.

94 The field effect transistor of Claim 90
wherein said **drain doping gradient region** surrounds
said **drain region**

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